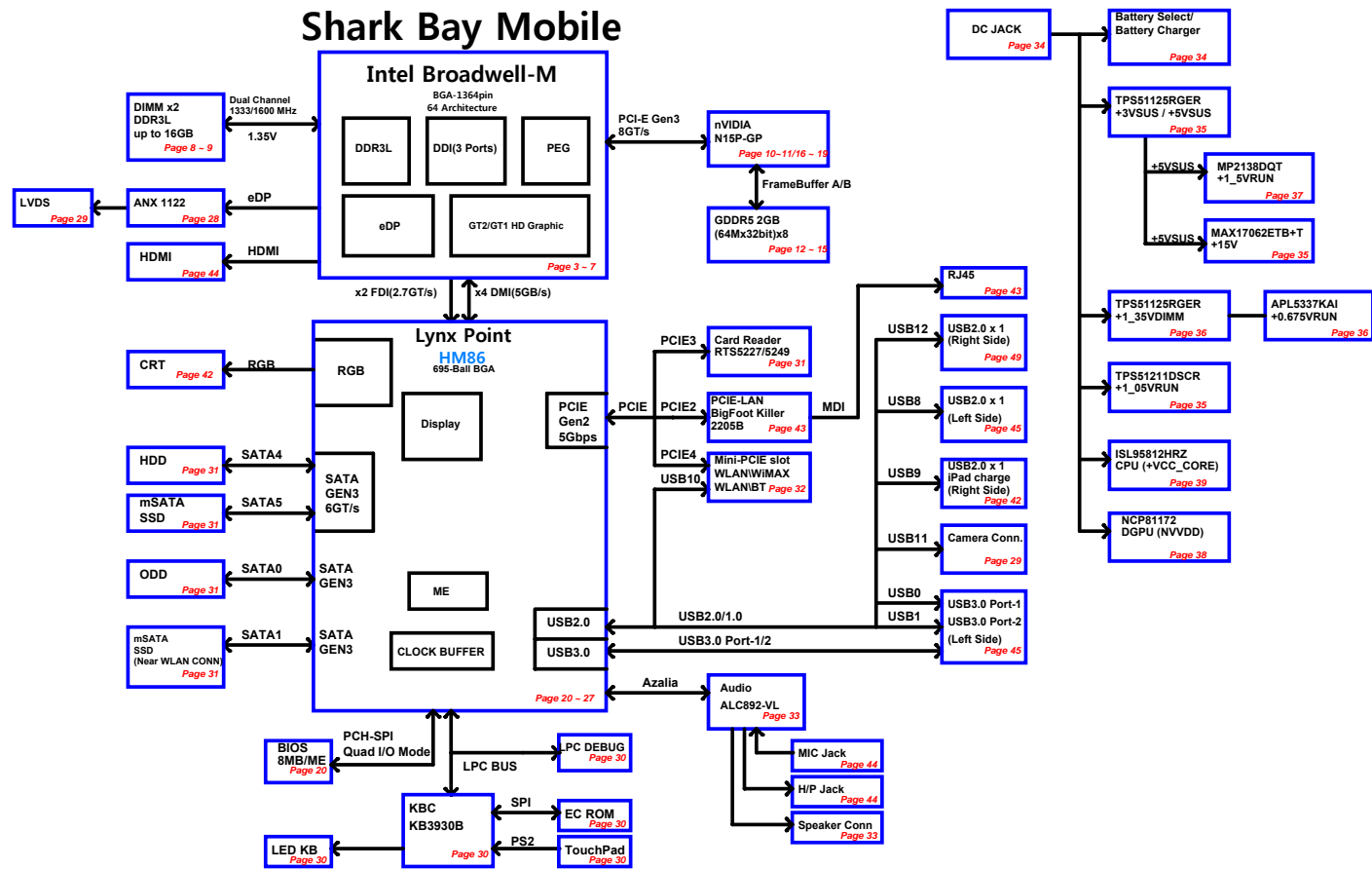


Shark Bay Mobile



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.8V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVD	0.6~1.2V(Vboot:0.9V)Core Voltage for nVIDIA N14E-GE DGPU	GPIO11_GPUVID
+3V3_NV	3.3V GPU I/O power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

POWER STATES

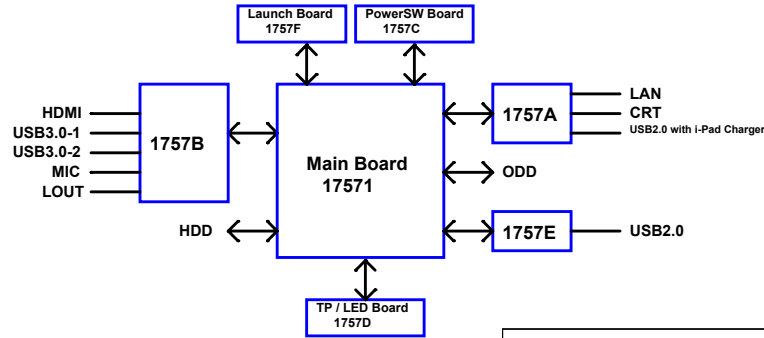
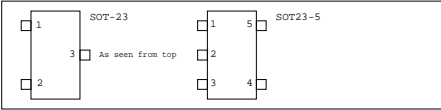
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

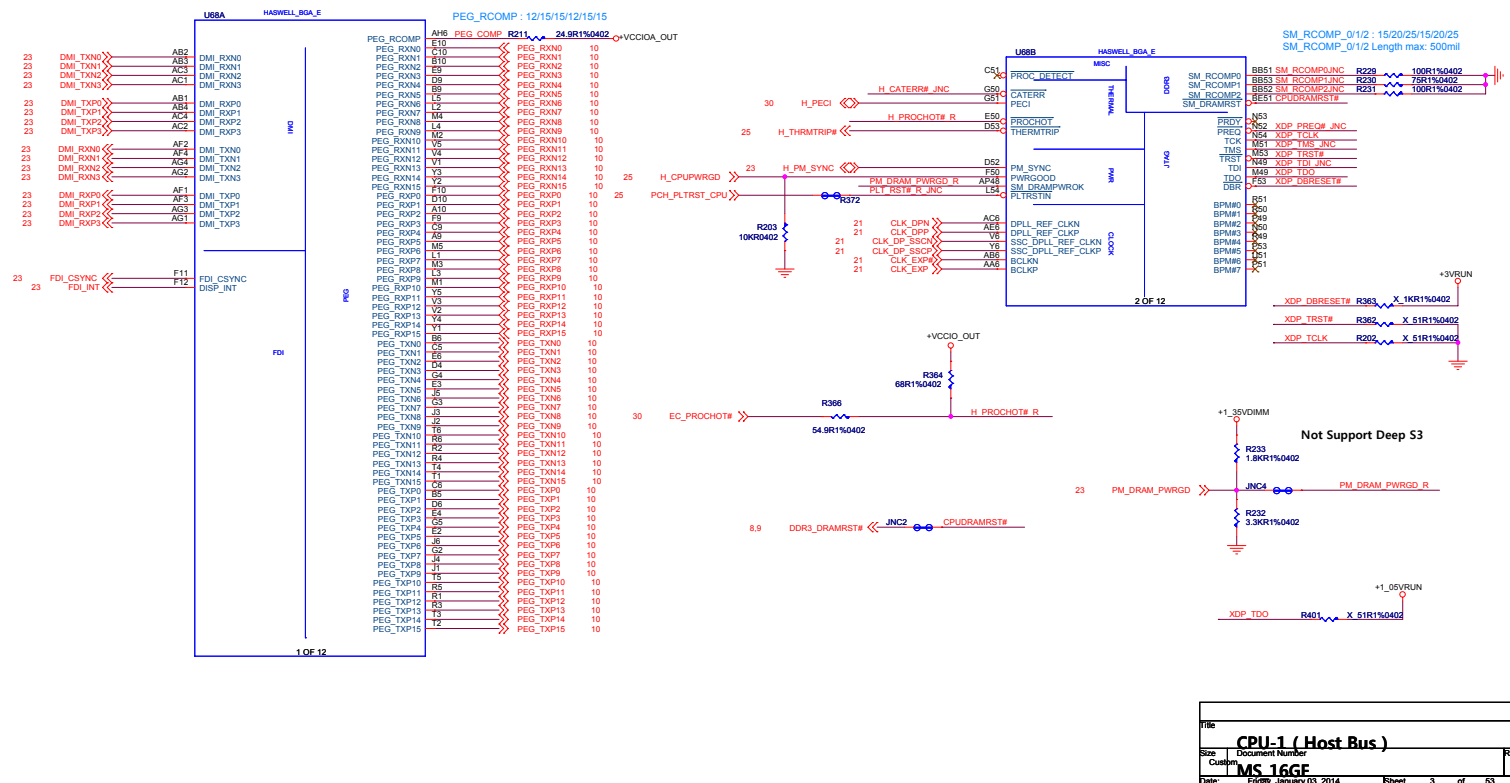
PCB Footprints



File	Platform
Size	Document Number
Customer	MS 16GE
Date	Fri9, January 03, 2014
Sheet	2 of 53
Rev	11

Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



Haswell (DDR3L)

SODIMM#B

SODIMM#A

HASWELL_BGA_E

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

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U88X

U88Y

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U88A

U88B

U88C

U88D

U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

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U88P

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U88W

U88X

U88Y

U88Z

U88A

U88B

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U88D

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U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

U88Q

U88R

U88S

U88T

U88U

U88V

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U88X

U88Y

U88Z

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U88B

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U88E

U88F

U88G

U88H

U88I

U88J

U88K

U88L

U88M

U88N

U88O

U88P

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U88V

U88W

U88X

U88Y

U88Z

U88A

U88B

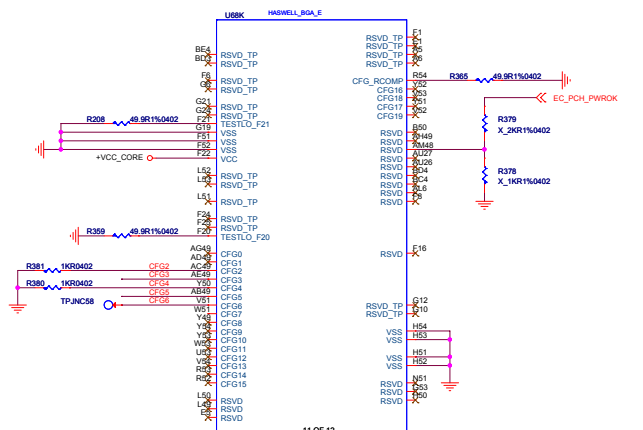
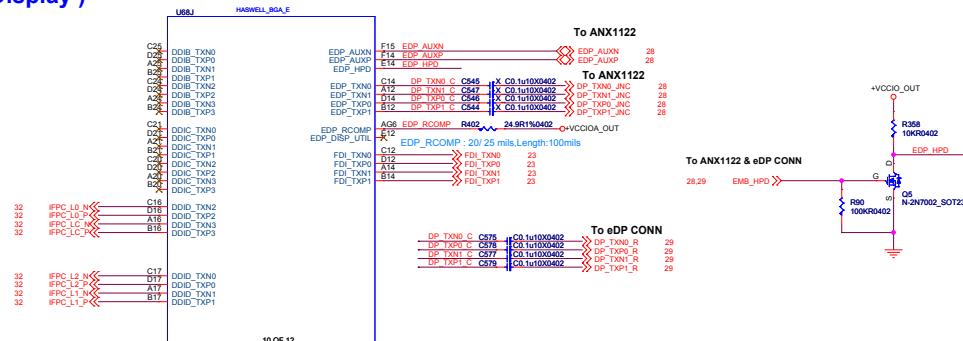
U88C

U88D

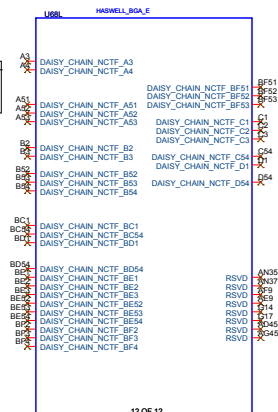
U88E

U88F

Haswell (Reserved)



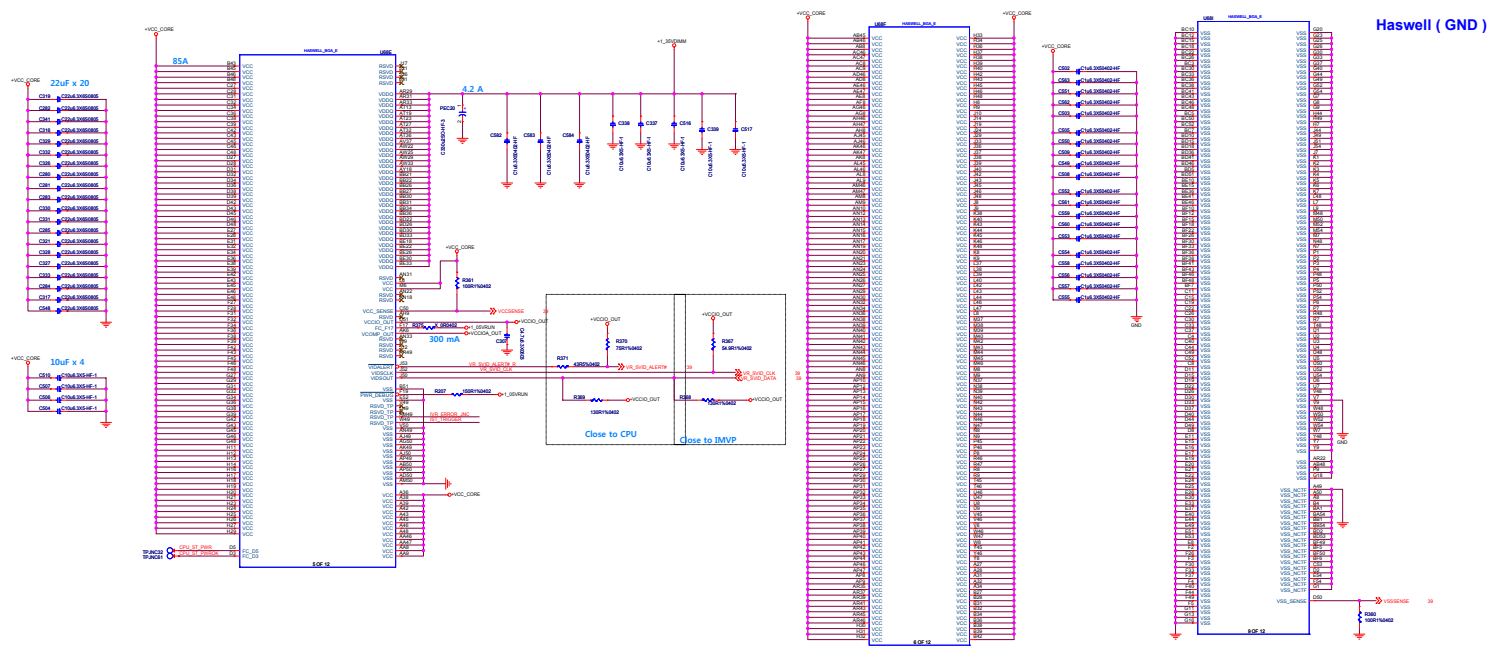
PCI Express* Static x16 Lane Numbers Reversed	
CFG2	1 = Normal operation 0 = Lane numbers reversed.
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface MSR (0x00000000) 0 = IA32_Debug_Interface_MSR (0xC600) output default setting overrides
xUP* enable	
CFG4	1 = Disabled 0 = Enabled
PCI Express* Bitification	
CFG8[6:0]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x4 PCI Express 11 = 1 x16 PCI Express
PEG DEFER TRAINING	
CFG7	0: (Default) PEG for immediate following xRES#ETB de assertion 1: PEG Wait for BIOS for training



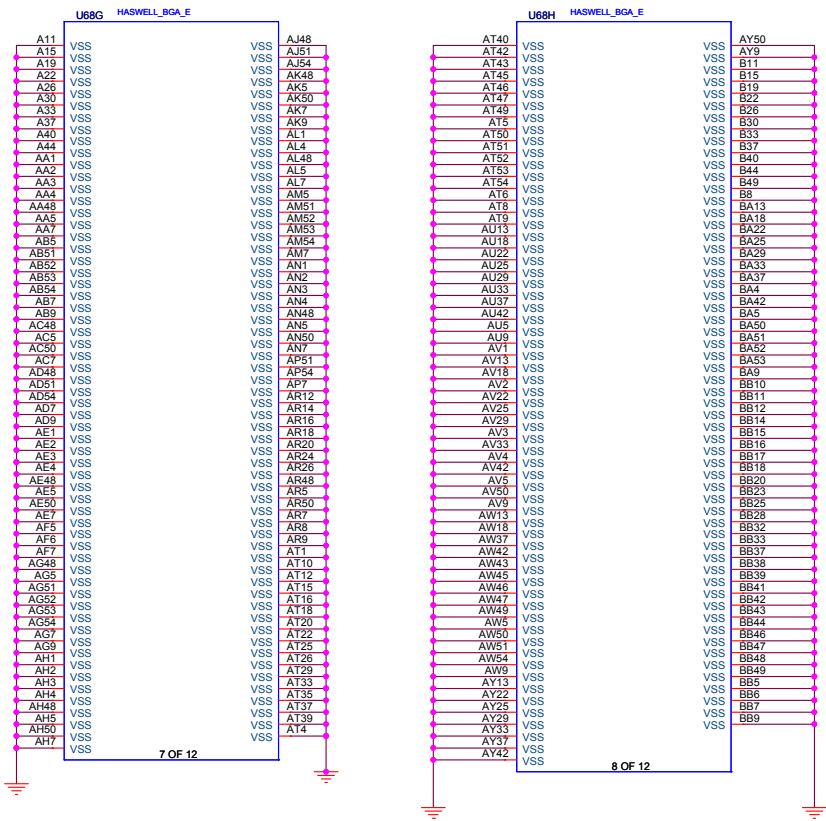
Title: **CPU-3 (Display/Reserved)**

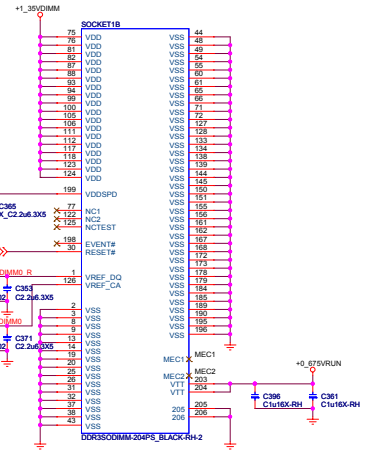
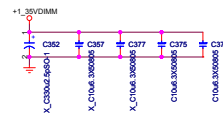
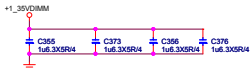
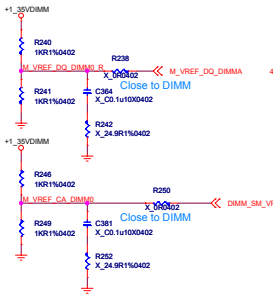
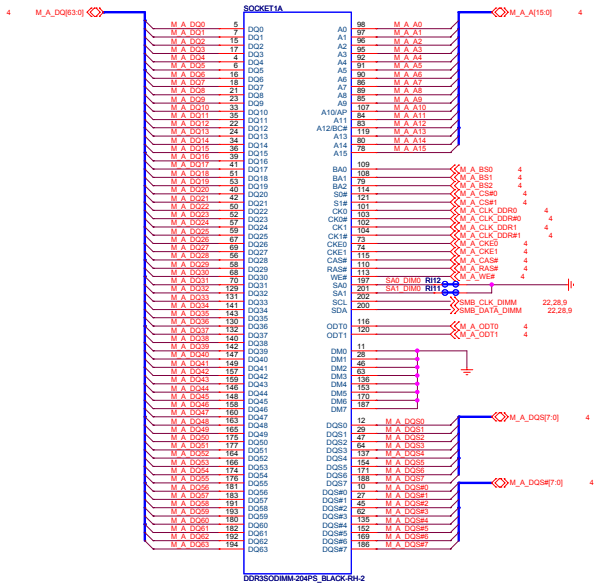
Size: Custom Document Number: MS 16GE Rev: 11

Date: Friday, January 03, 2014 Sheet: 5 of 53



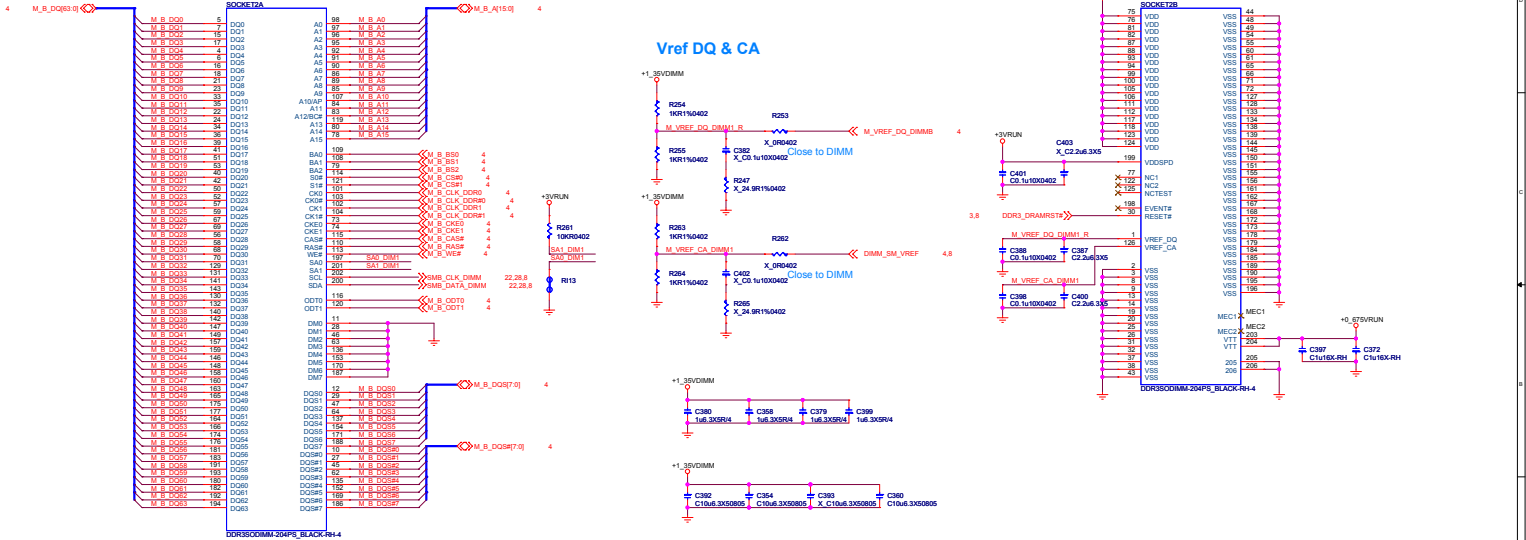
Haswell (GND)



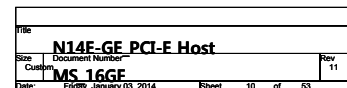
SODIMM#A

File		DDR3L SODIMM 0		Rev	11
Size	Document Number				
Custom	MS 16GF				
Date	Fri 09 January 03, 2014	Sheet	8	of	53

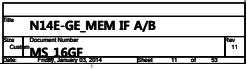
SODIMM#B



The diagram shows the timing relationship between three signals: DGPU_PWRGD (green), PEX_CLKREQ# (blue), and GPU_CLKREQ# (red). DGPU_PWRGD is a pulse-width modulated signal. PEX_CLKREQ# is a periodic square wave. GPU_CLKREQ# is a single pulse. The circuit includes a resistor RC398, a 2M90452 component, and two N-2N7002LT1G_SOT23-RH MOSFETs (Q6 and Q13). The timing parameters are listed as 17, 19, 25, 30.



1



)



)



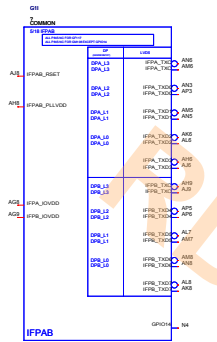
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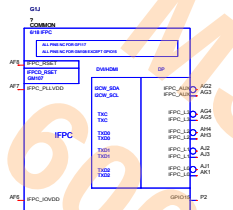
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N14E-GE(Display IF)

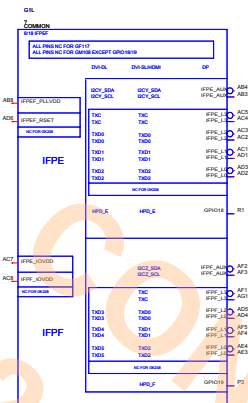
IFP A/B LVDS Dual Link



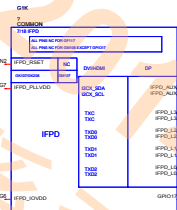
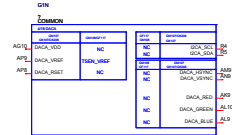
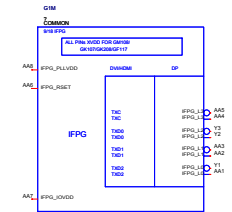
IFP C Native HDMI OR DP

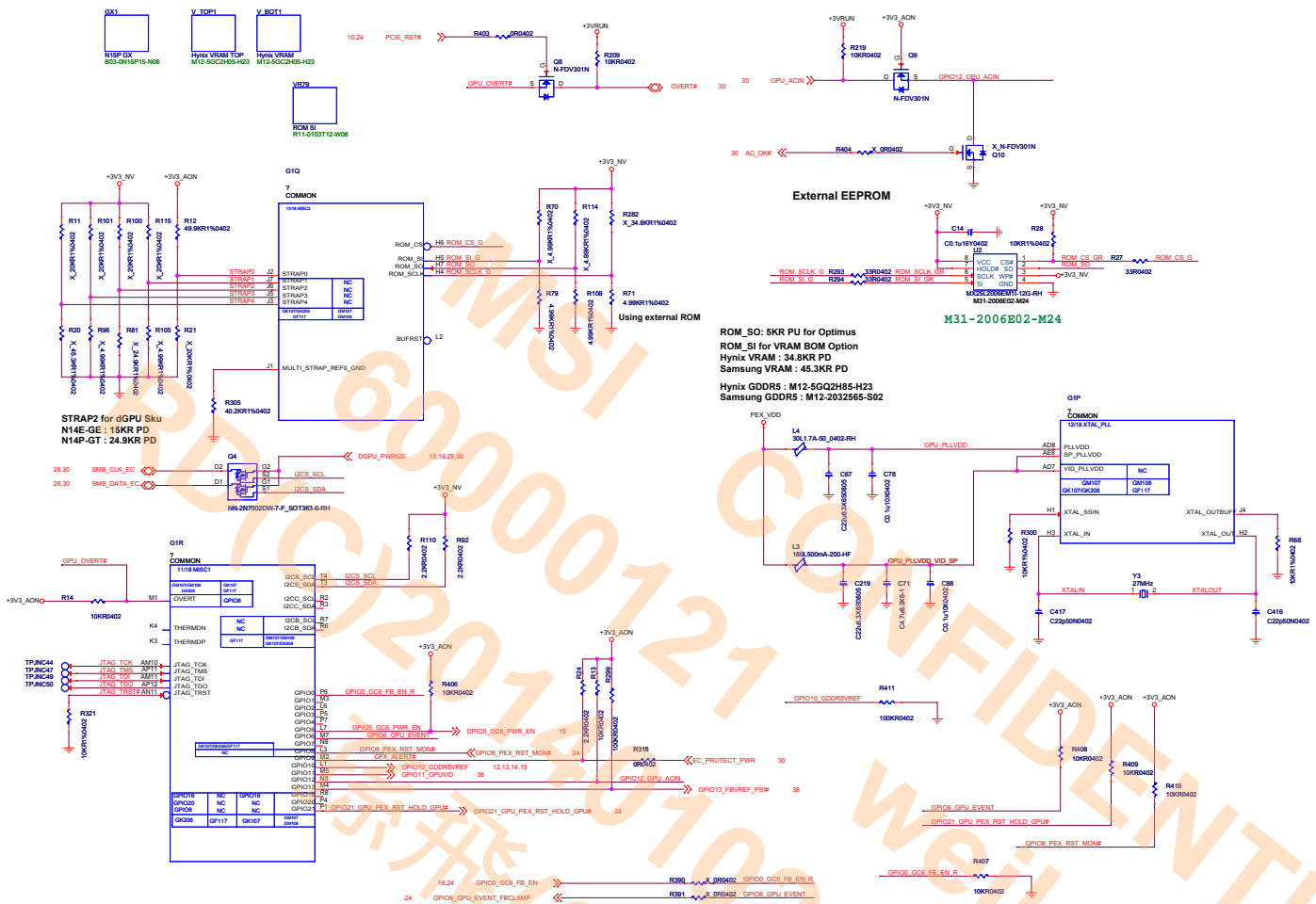


IFP E/F Dual Link TMDS DVI-I

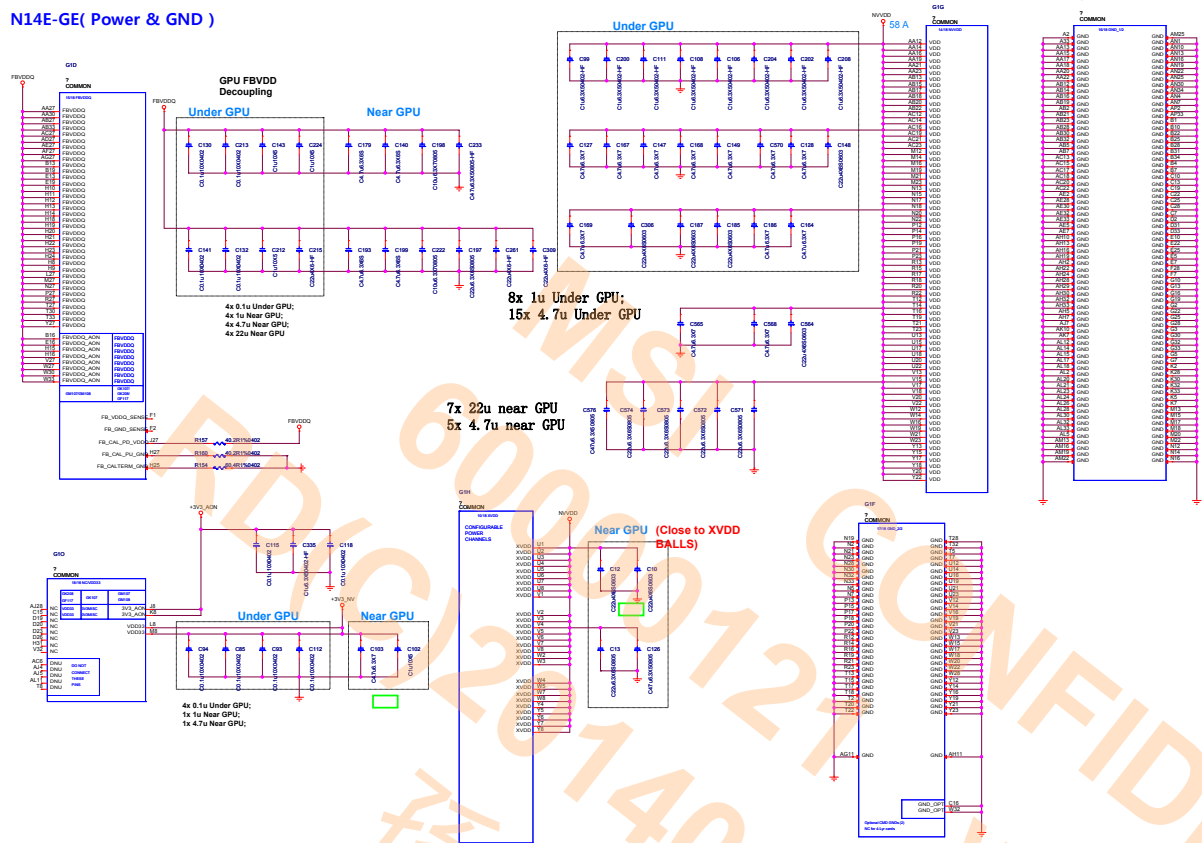


DAC A VGA

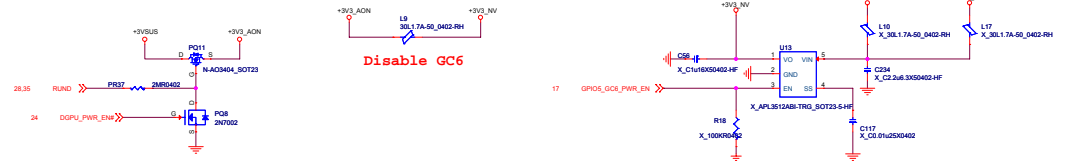




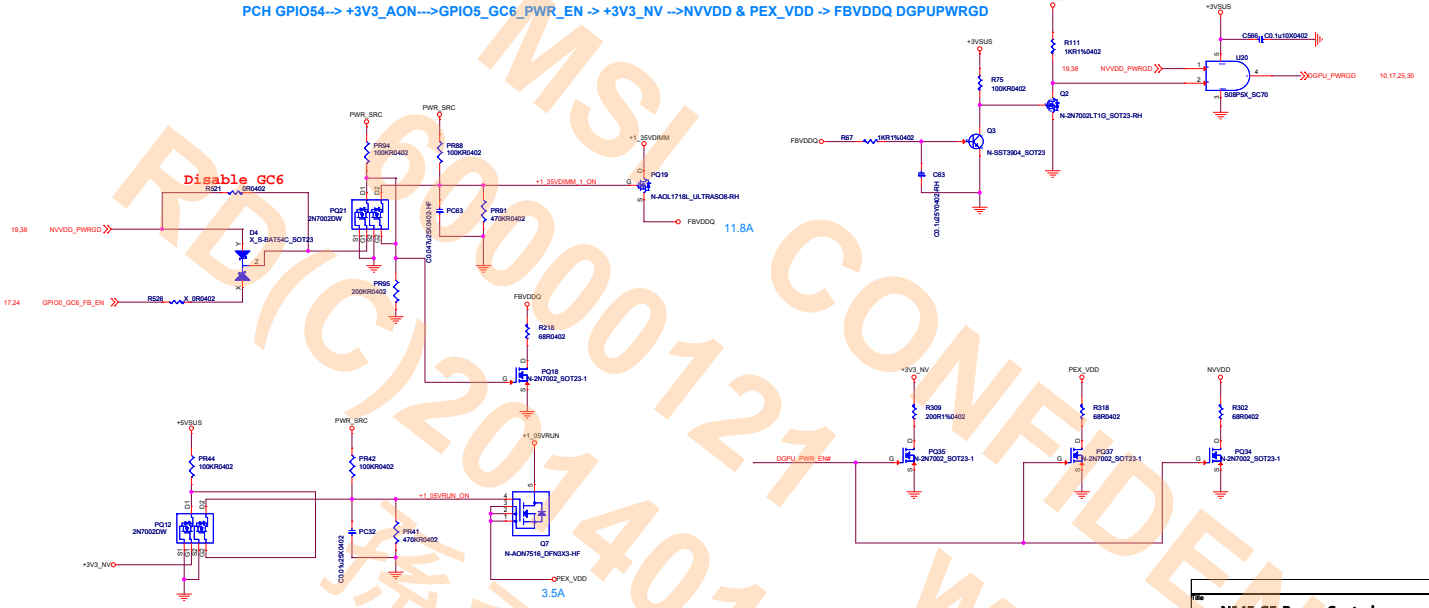
N14E-GE(Power & GND)



N15P-GE(Power Control)

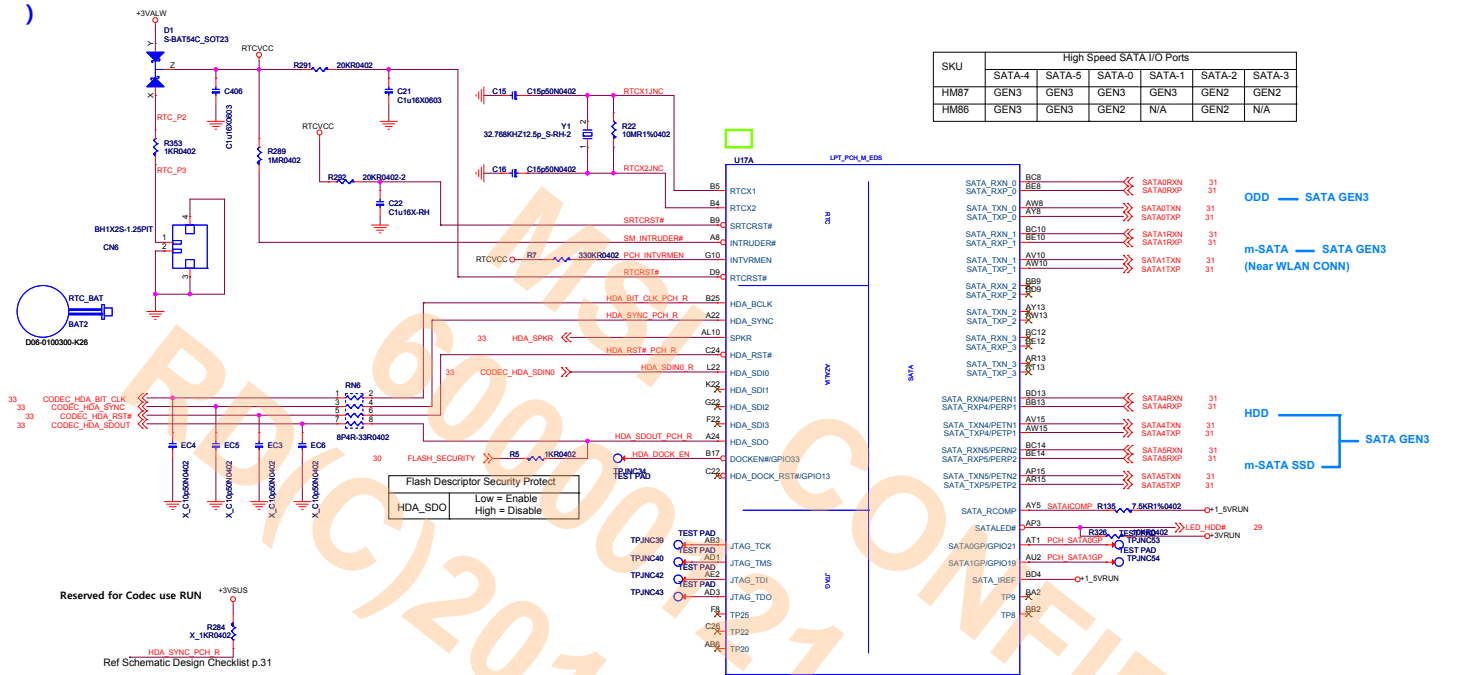


PCH GPIO54--> +3V3_AON-->GPIO5_GC6_PWR_EN -> +3V3_NV -->NVVDD & PEX_VDD -> FBVDDQ DGPUPWRGD

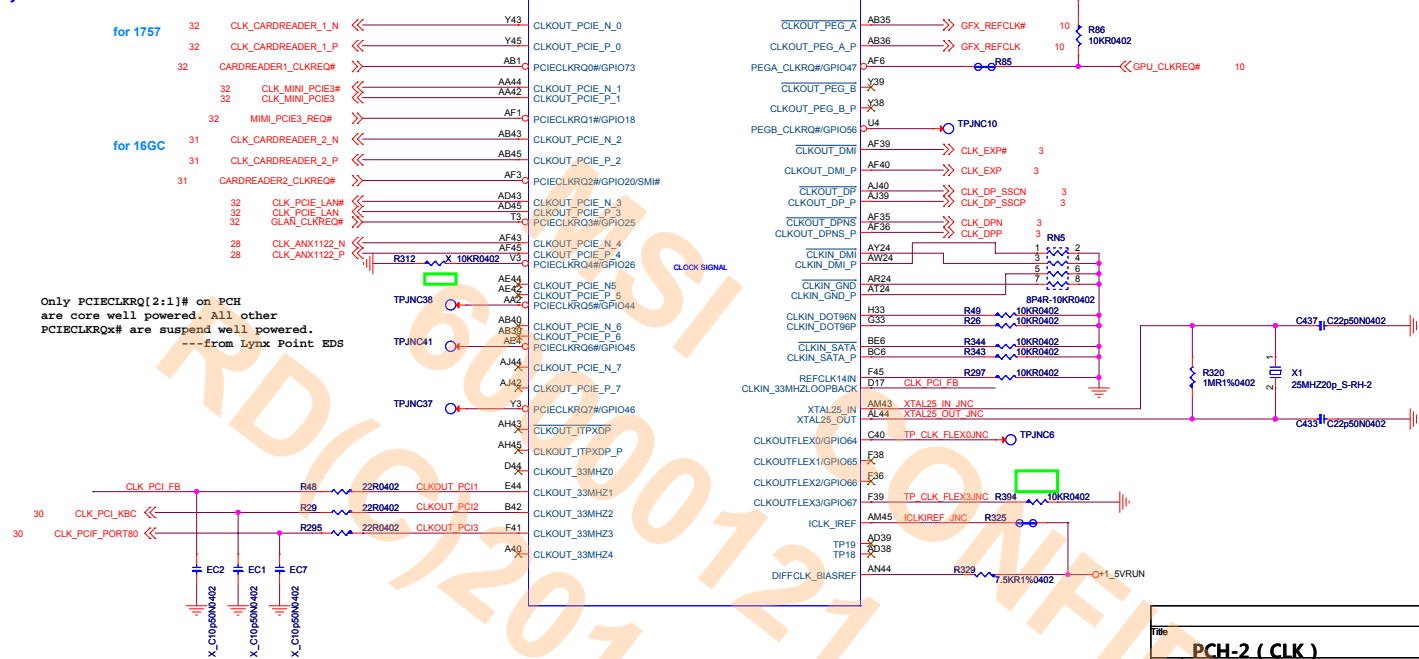


Rev	1	N14E-GE Power Control		Rev	11
Doc	MS 16GE			Doc	
File	PowerControl_2024			File	

Lynx Point (HDA,JTAG,SATA)

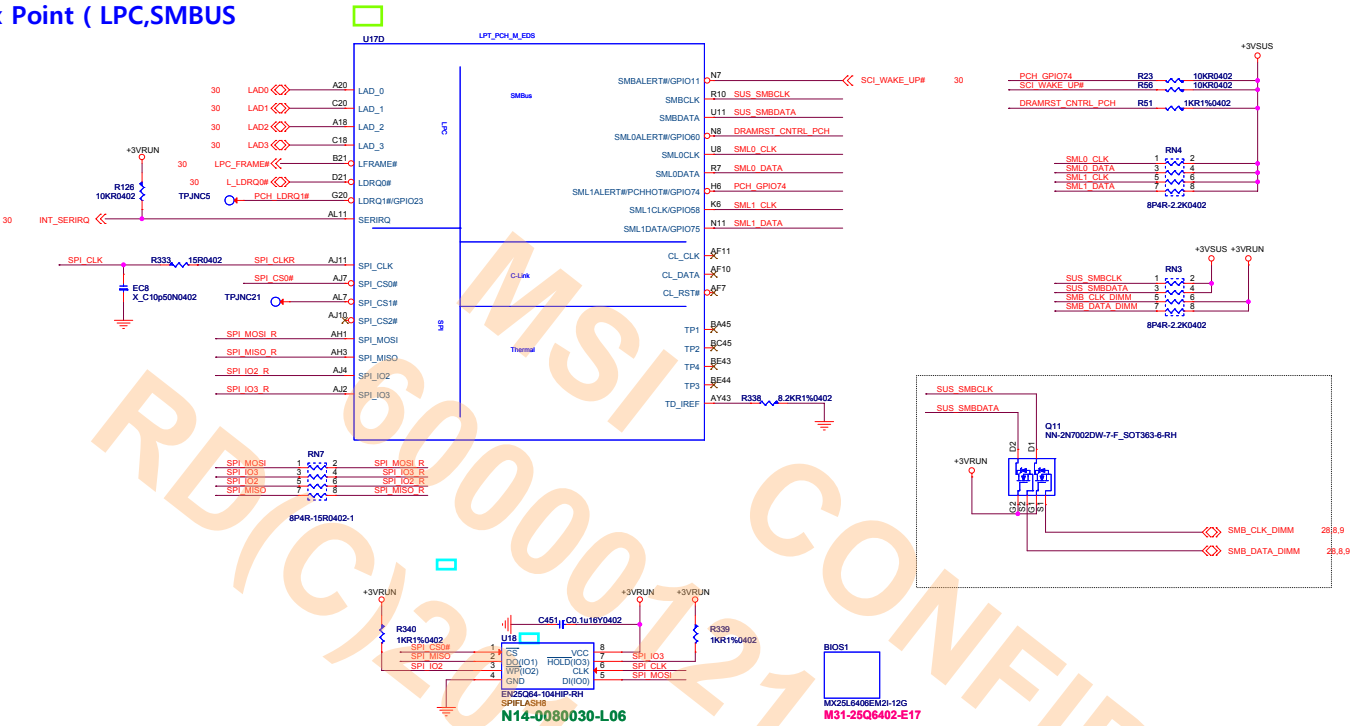


Lynx Point (Clock)



Title		PCH-2 (CLK)		Rev		11	
Size	Document Number						
Custom	MS 16GE						
Date:	Friday, January 03, 2014	Sheet	21	of	53		

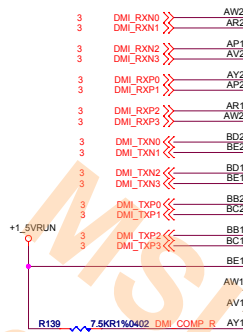
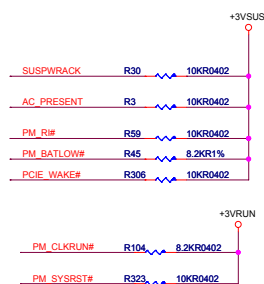
Lynx Point (LPC,SMBUS)



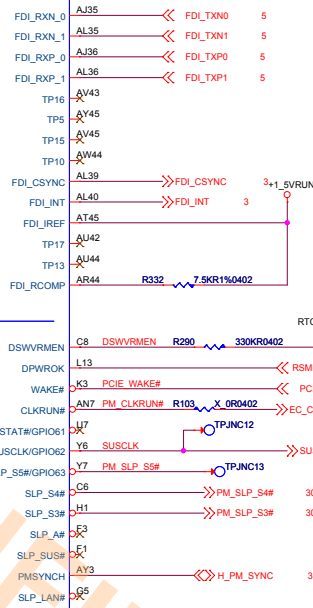
Title		PCH-3 (LPC,SMBUS)	
Size	Document Number	MS 16GE	Rev 11
Customer	Date	Friday, January 03, 2014	Sheet 22 of 63

Lynx Point (DMI,FDI)

)



U17B LPT_PCH_M_EDS



APWROK
not supporting Intel AMT , it can be connected to PWROK

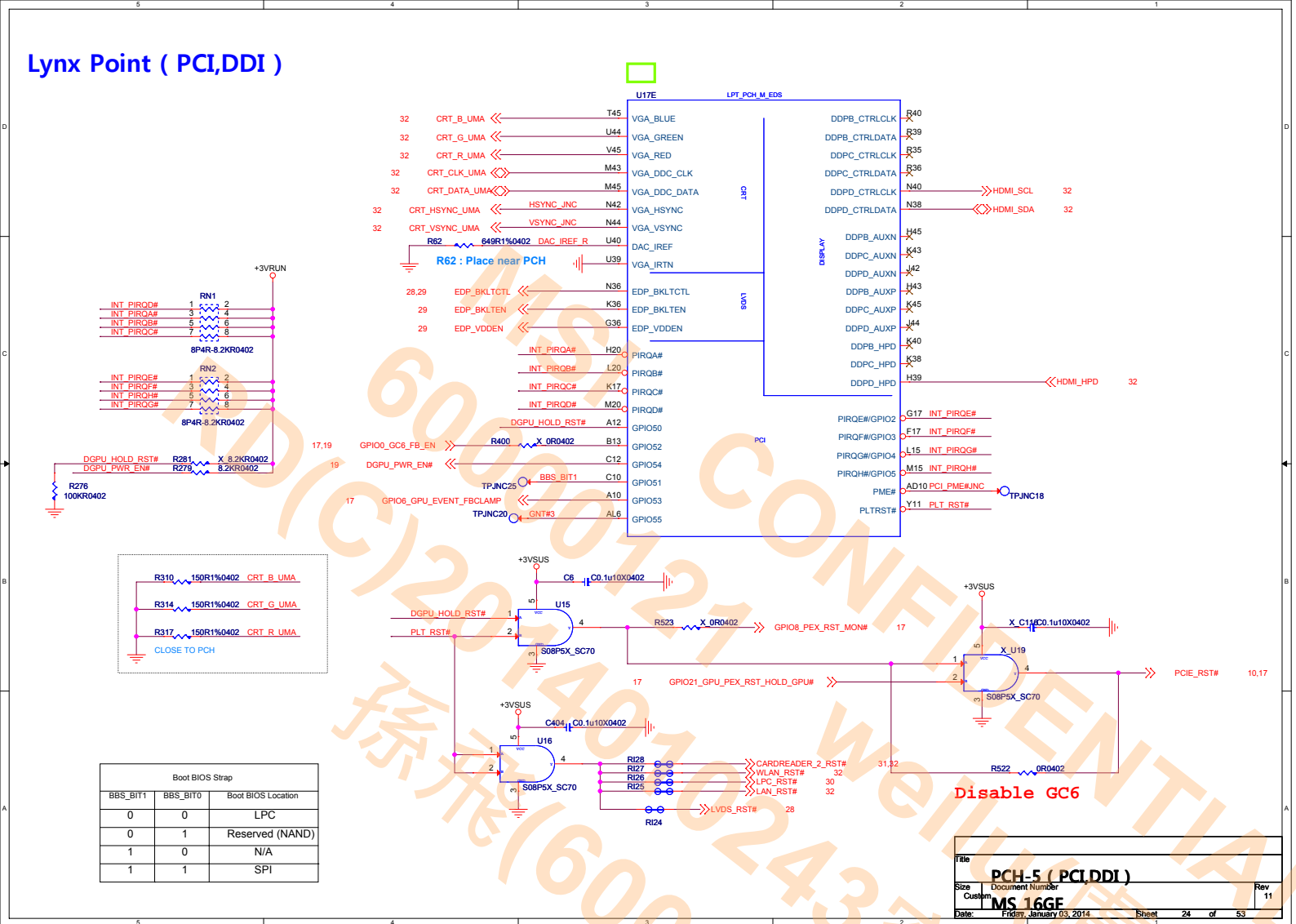
GPIO31 : If not used,require pull up +3VSUS

DSWODVREN - On Die DSW VR Enable
HIGH : Enable internal 1.05V regulator
LOW : Disable

DPWROK
Without deep s4/s5 support tied together with RSMRST#

Title			PCH-4 (DMI,FDI)	
Size	Document Number	MS 16GE		Rev
Customer				11
Date:	Fri, January 03, 2014	Sheet	23	of 53

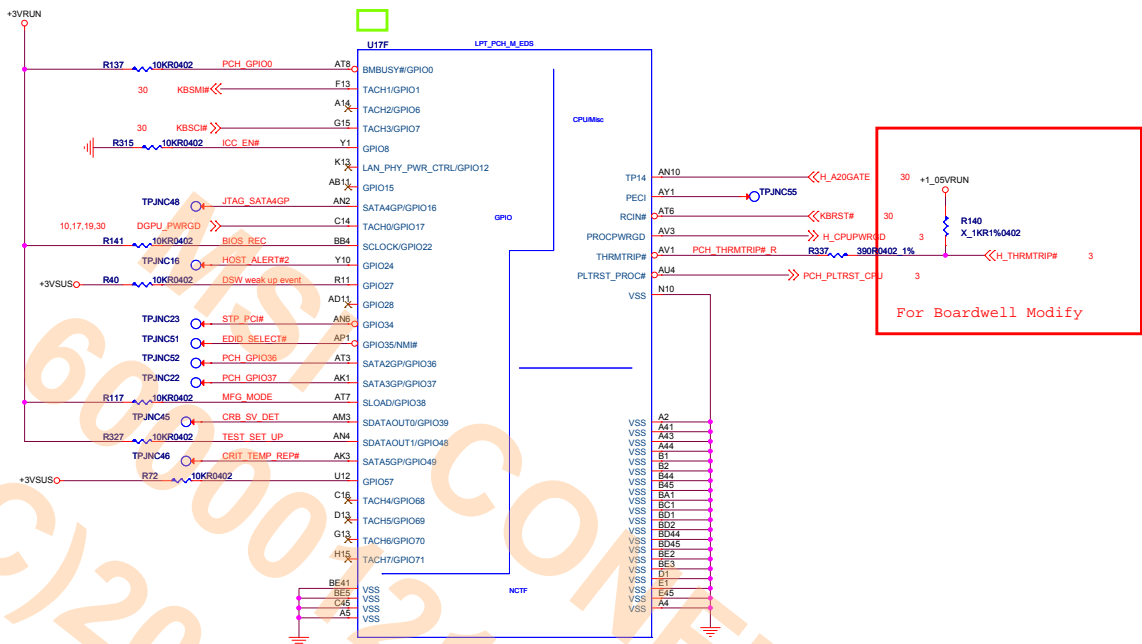
Lynx Point (PCI,DDI)



Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



Title		Rev
PCH-6 (GPIO,MISC)		
Size	Document Number	11
Customer	MS 16GF	
Date:	Friday, January 03, 2014	Sheet 26 of 53

Lynx Point (PCIE,USB)

Card Reader for 1757

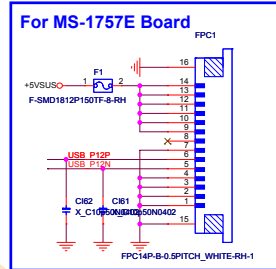
LAN

Card Reader for 16GC

WLAN

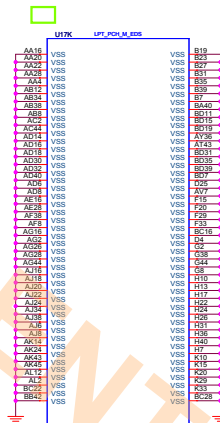
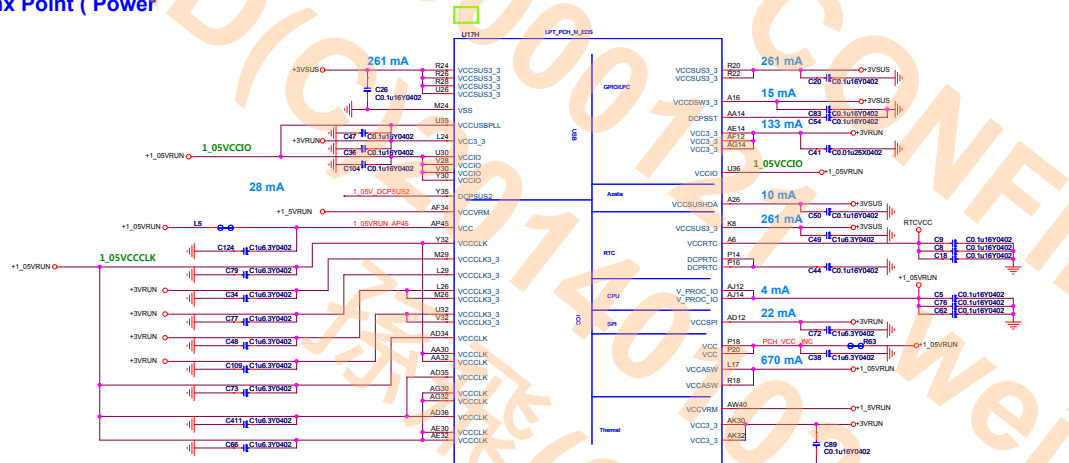
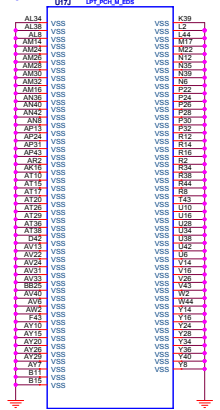
Close to device

USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	(16GCB/1757B)
1	2	USB 3.0 Port 2	(16GCB/1757B)
2			NC
3			NC
4			NC
5			NC
6			NC
7			NC
8		USB 2.0 Port	(16GCB)
9		USB 2.0 Port	(16GCA/1757A)
10		WLAN	
11		WebCam	
12		USB 2.0 Port	(1757E)
13			NC
	3		NC
	4		NC
	5		NC
	6		NC

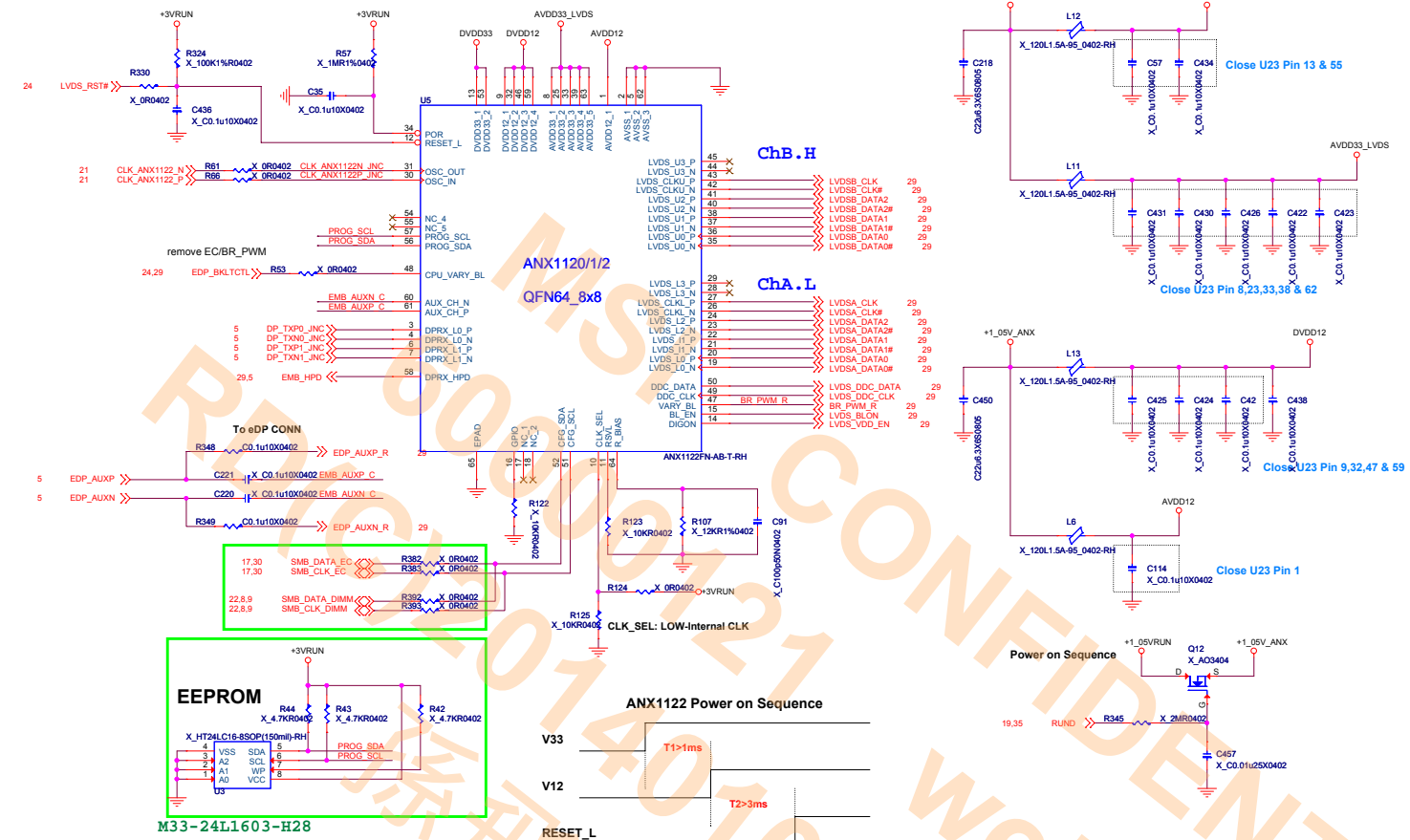


File	PCH-7 (PCIE,USB)		
Doc	Document Number		Rev 11
Date	17 May 2014	Sheet	28 of 53

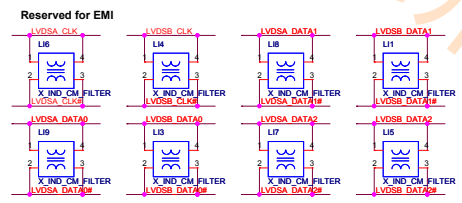
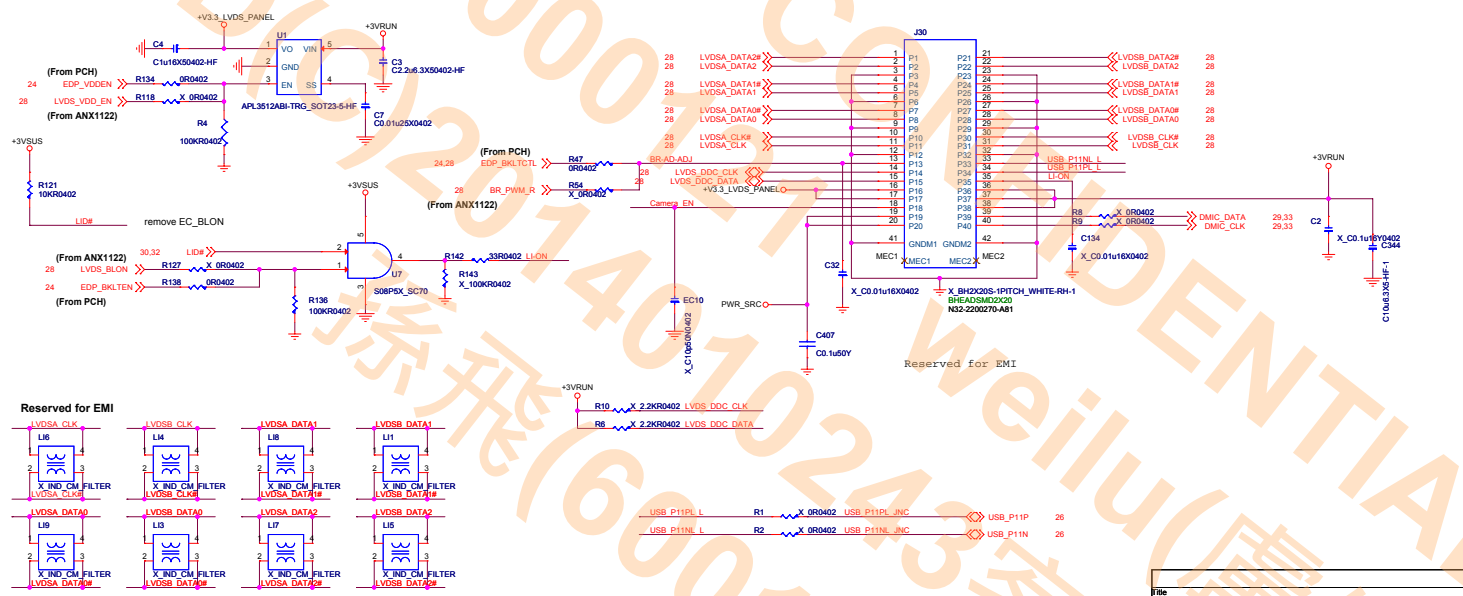
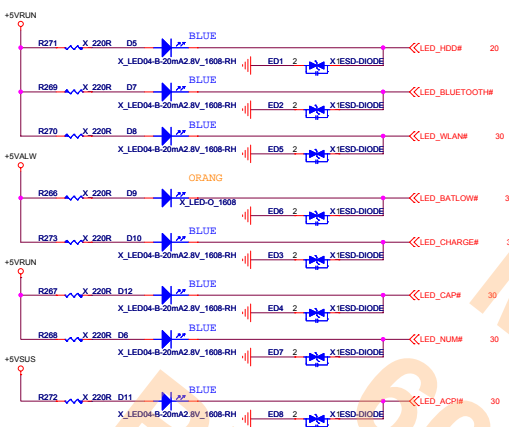
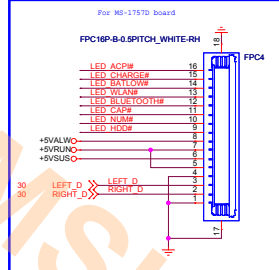
Lynx Point (Power)



eDP to LVDS



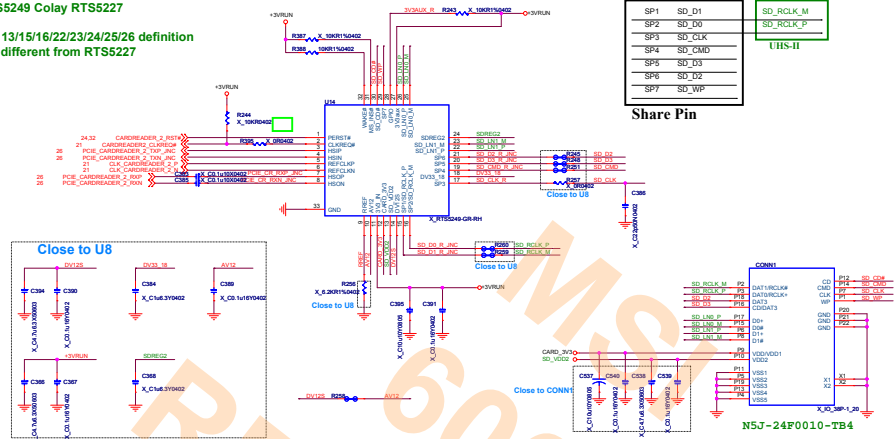
eDP to LVDS (ANX1122)		
Size	Document Number	Rev
MS 16GE		11
Date	File	Sheet
2014	Jan 03	26 of 53



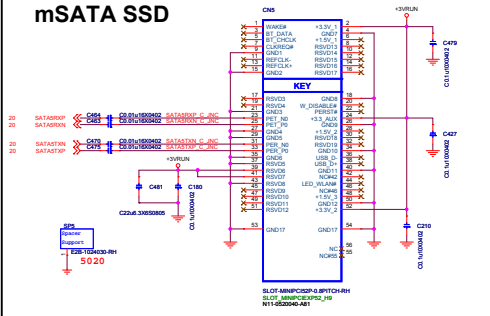


CardReader
RTS5249 Colay RTS5227

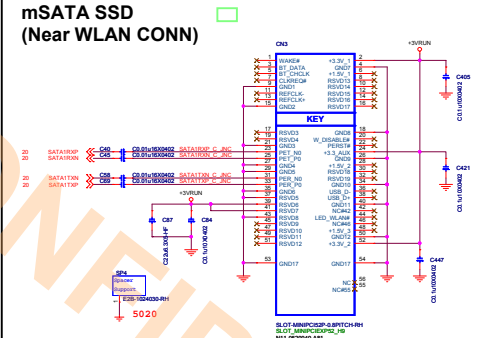
Pin 13/15/16/22/23/24/25/26 definition
are different from RTS5227



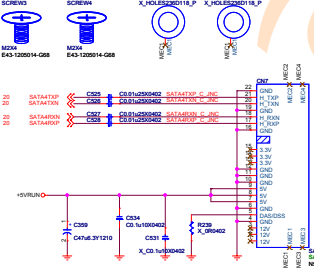
mSATA SSD



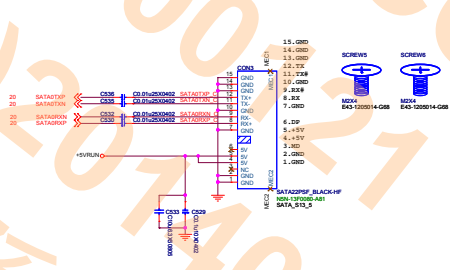
mSATA SSD
(Near WLAN CONN)



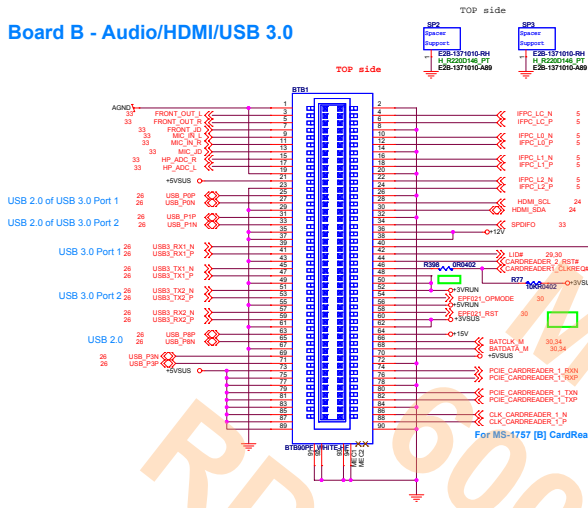
SATA HDD



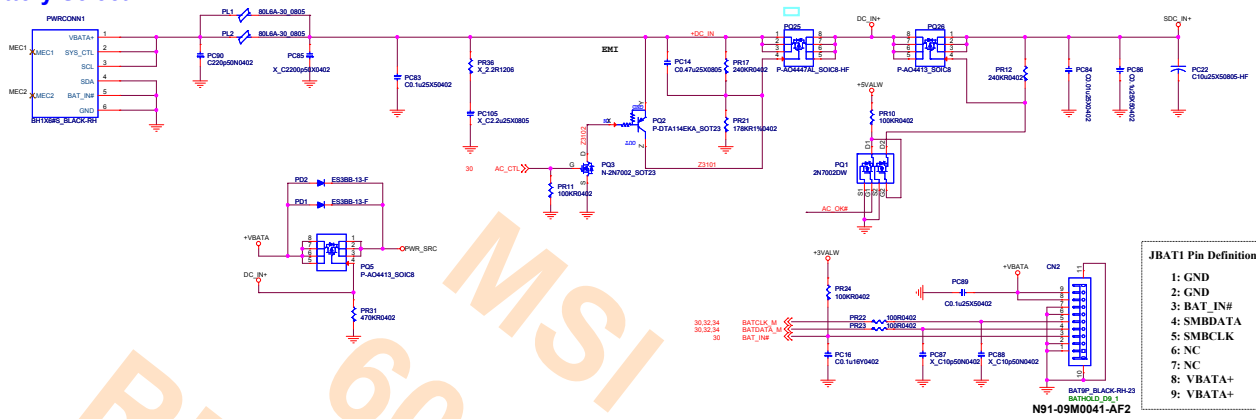
SATA ODD



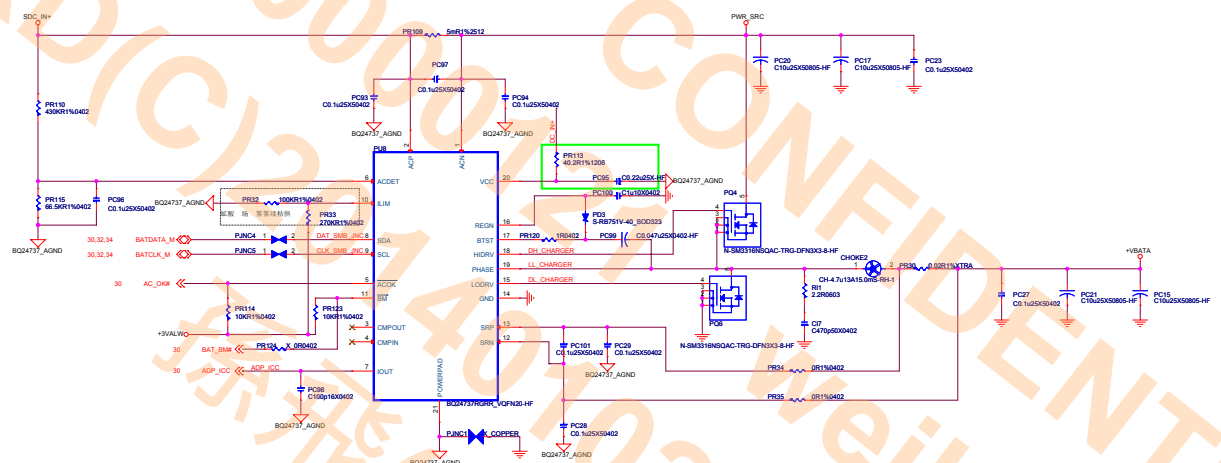
Board B - Audio/HDMI/USB 3.0



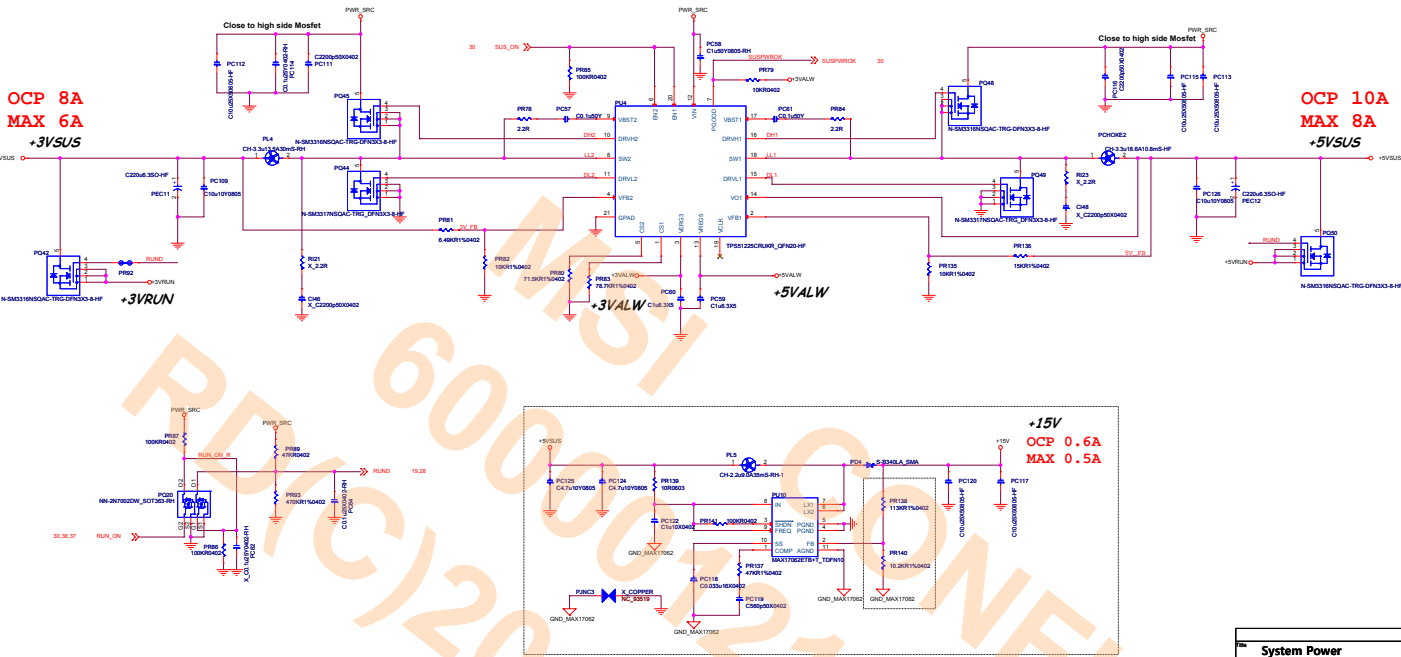
Battery Select



Battery Charger

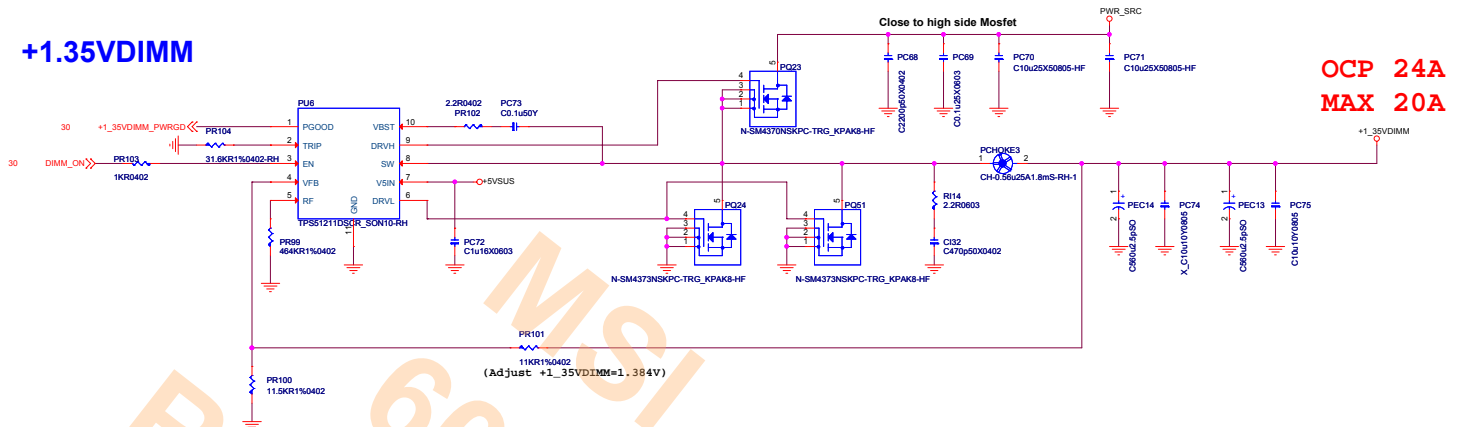


System Power

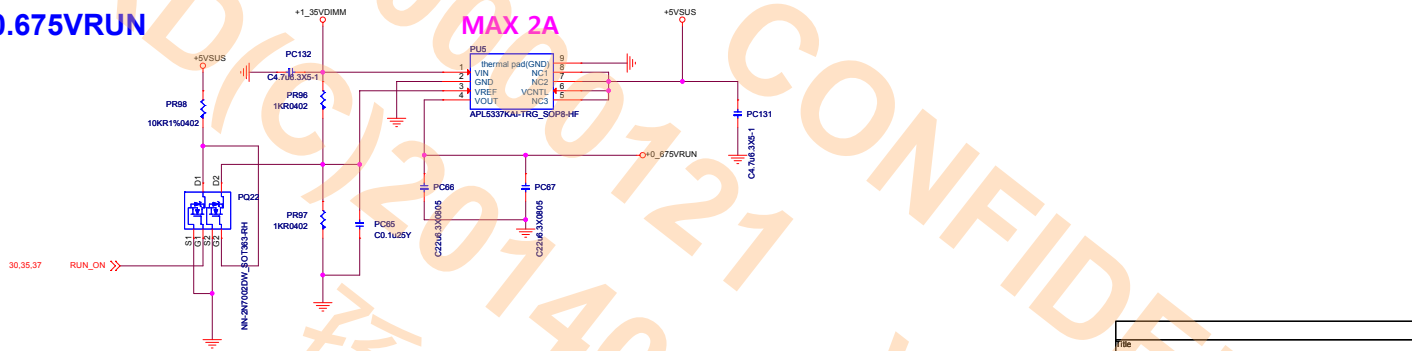


Rev	System Power
1	MS 166F
Date	2014.01.15
Drawn	weilu
Checked	weilu
Page	11

+1.35VDIMM

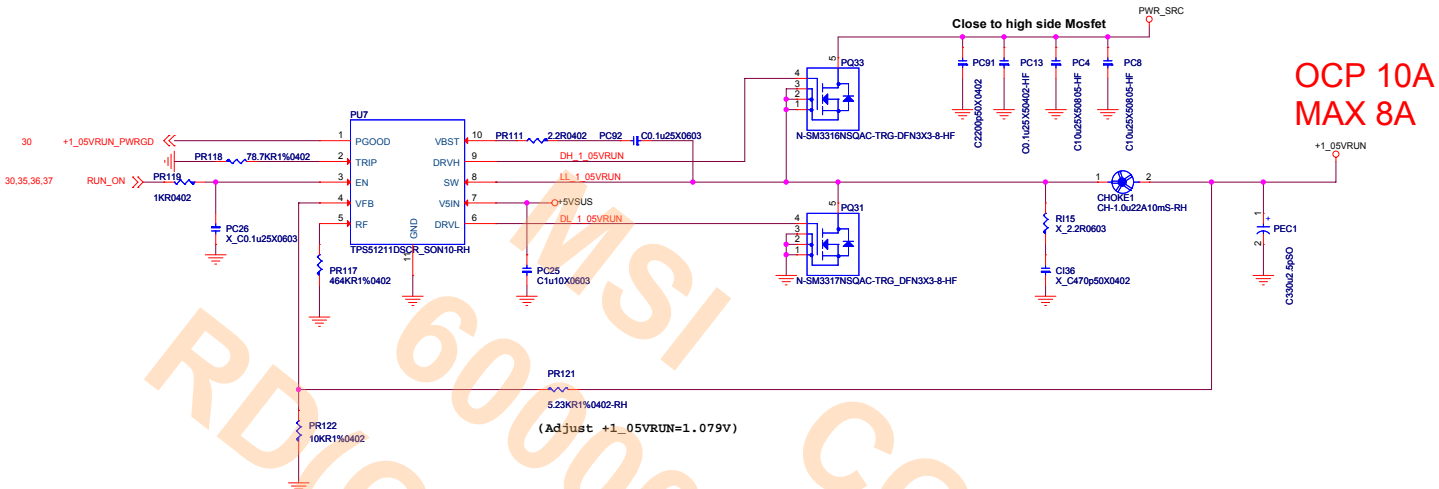


+0.675VRUN

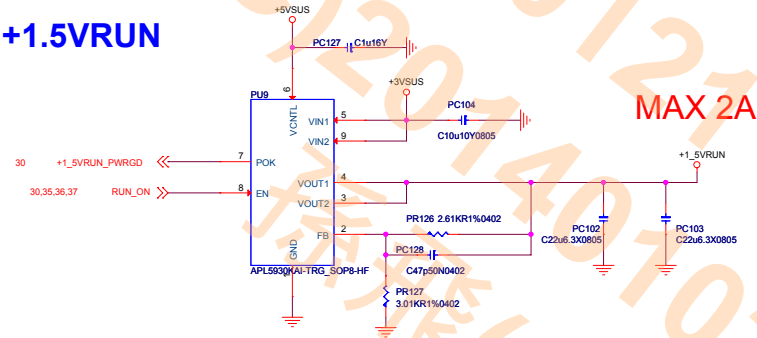


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Size	1000000	11	11
Customer	MS 16GE		
Date	2014-03-03	Sheet	38 of 53

+1.05VRUN



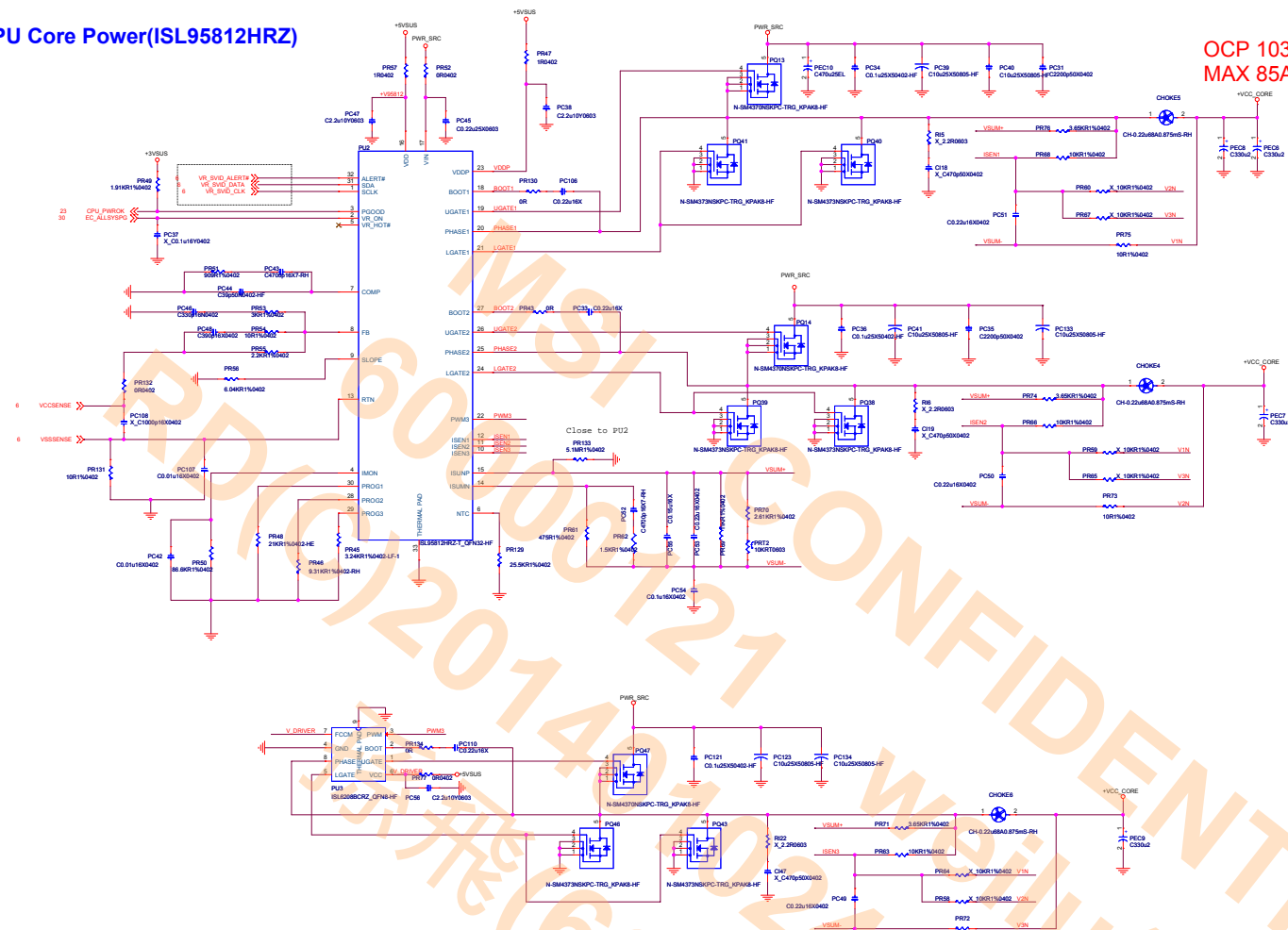
+1.5VRUN



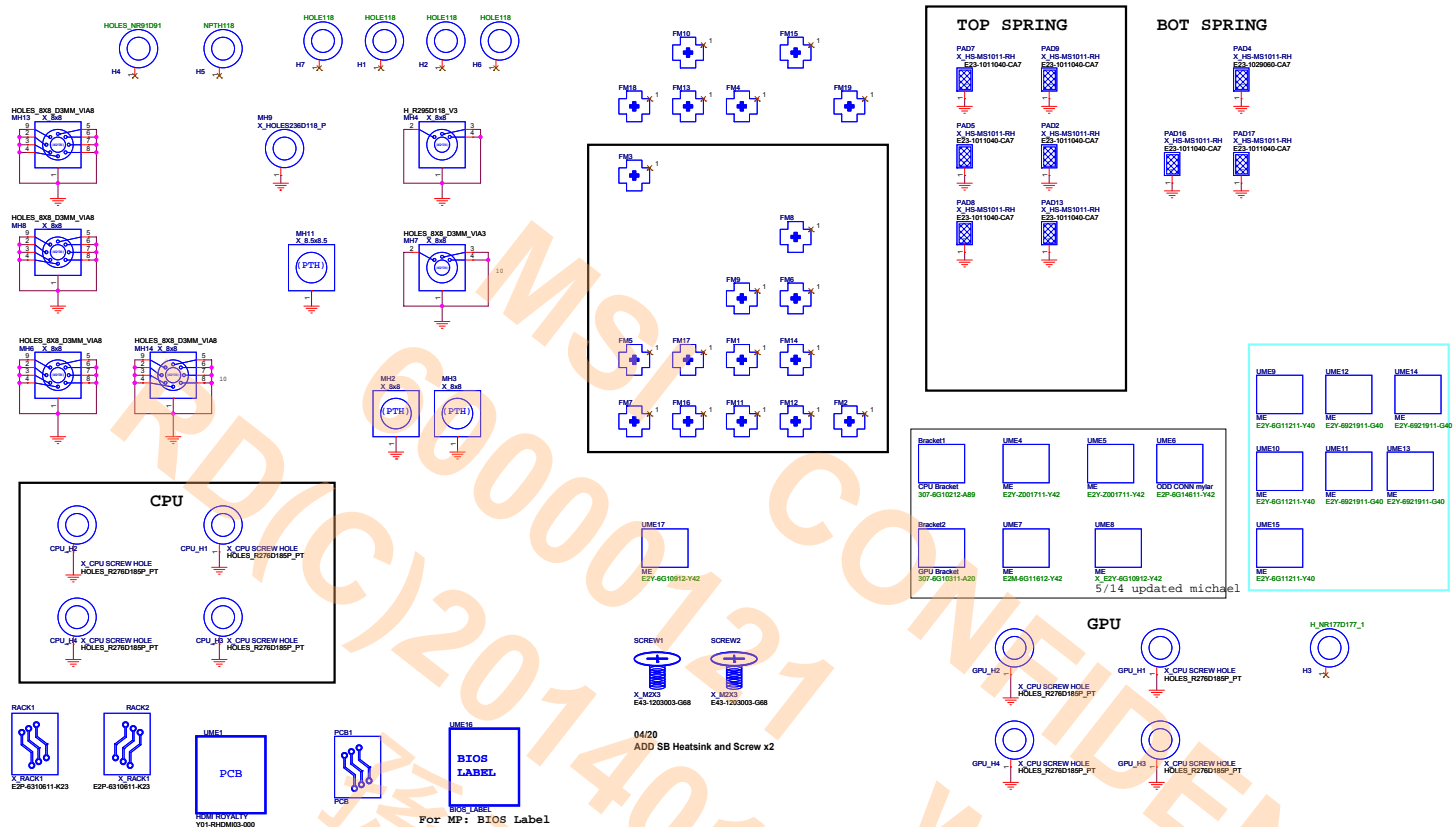
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Size	Document Number		
Customer	MS 16GE		
Date	Friday, January 03, 2014	Sheet	37 of 53

CPU Core Power(ISL95812HRZ)

OCP 103A
MAX 85A



Rev	Rev	Rev
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2	2	2
3	3	3
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Top Spring

PAD6
X_HS-MS1011-RH
E23-1011040-CA7



PAD11
X_HS-MS1011-RH
E23-5551040-CA7

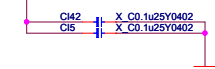


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X_HS-MS1011-RH
E23-5551040-CA7

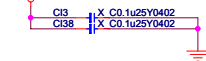


PWR_SRC

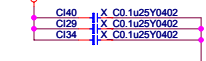
Close to PQ31, PQ34



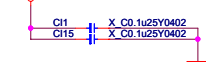
SDC_IN+



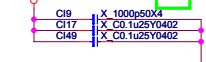
+5VSUS



PWR_SRC



+5VRUN



BOT Spring

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X_HS-MS1011-RH
E23-1011040-CA7



PAD15
X_HS-MS1011-RH
E23-1011040-CA7



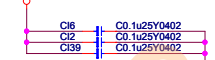
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E23-5551040-CA7



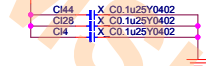
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E23-5551040-CA7



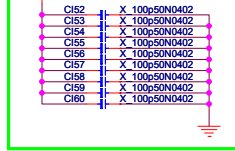
+VBATA



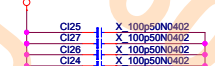
+3VRUN



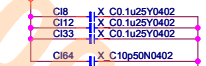
+1_35VDIMM



FBVDDQ



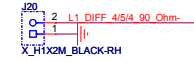
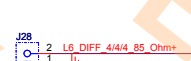
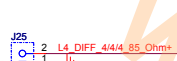
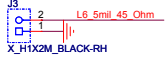
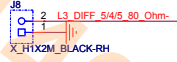
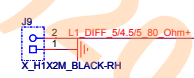
+3VSUS



45 OHM

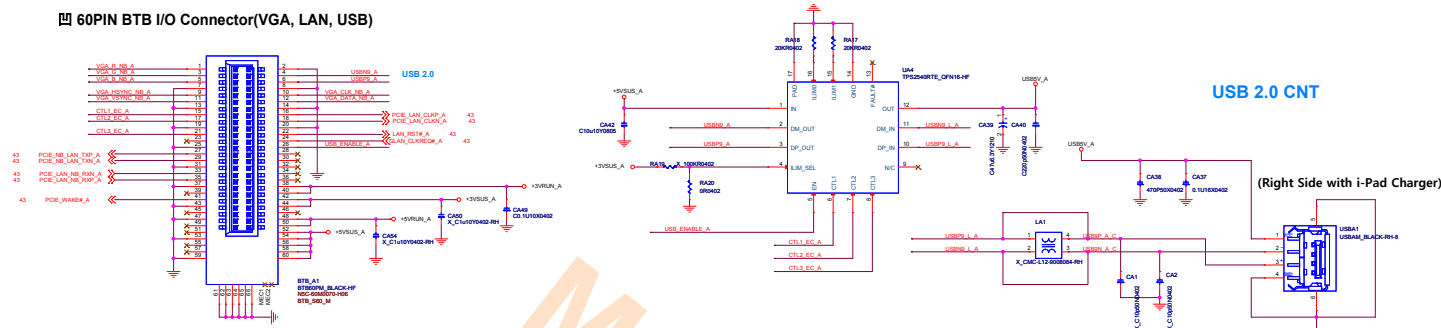


80 OHM



Title				
Size		EMI Document Number		Rev 11
Customer		MS 16GE		
Date:	Friday, January 03, 2014		Sheet	41 of 53

四 60PIN BTB I/O Connector(VGA, LAN, USB)

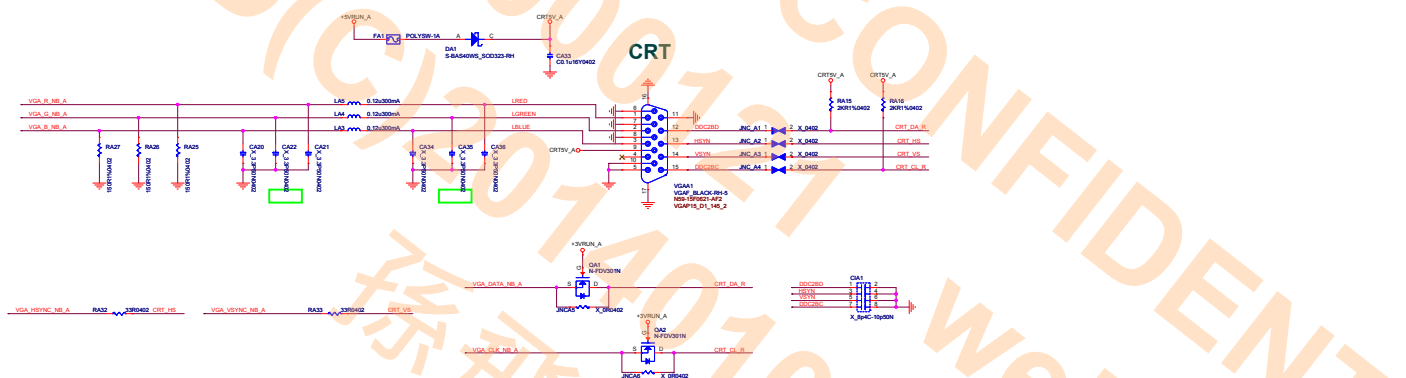


BTB STANDOFF (16GMA)

SCREW HOLE

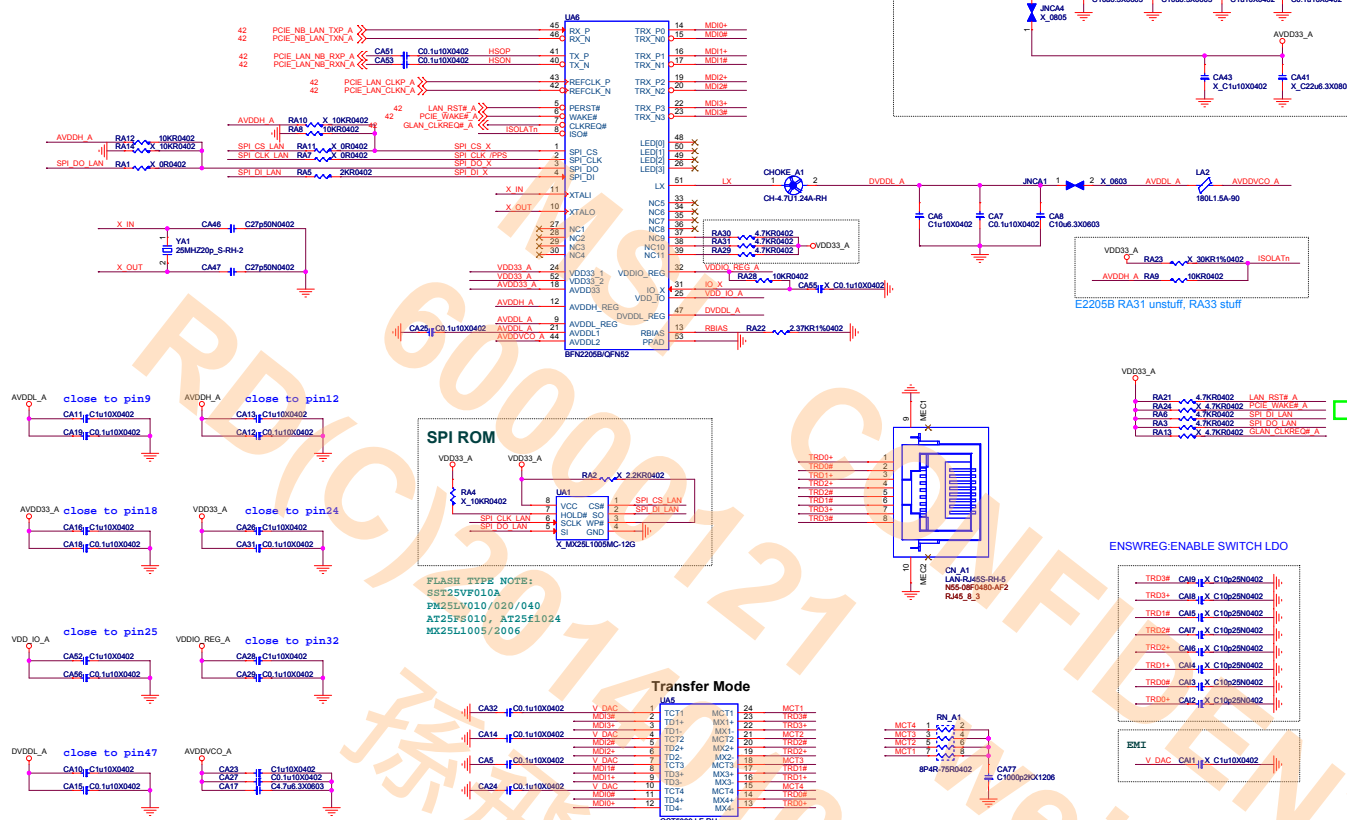


PCB_VSB



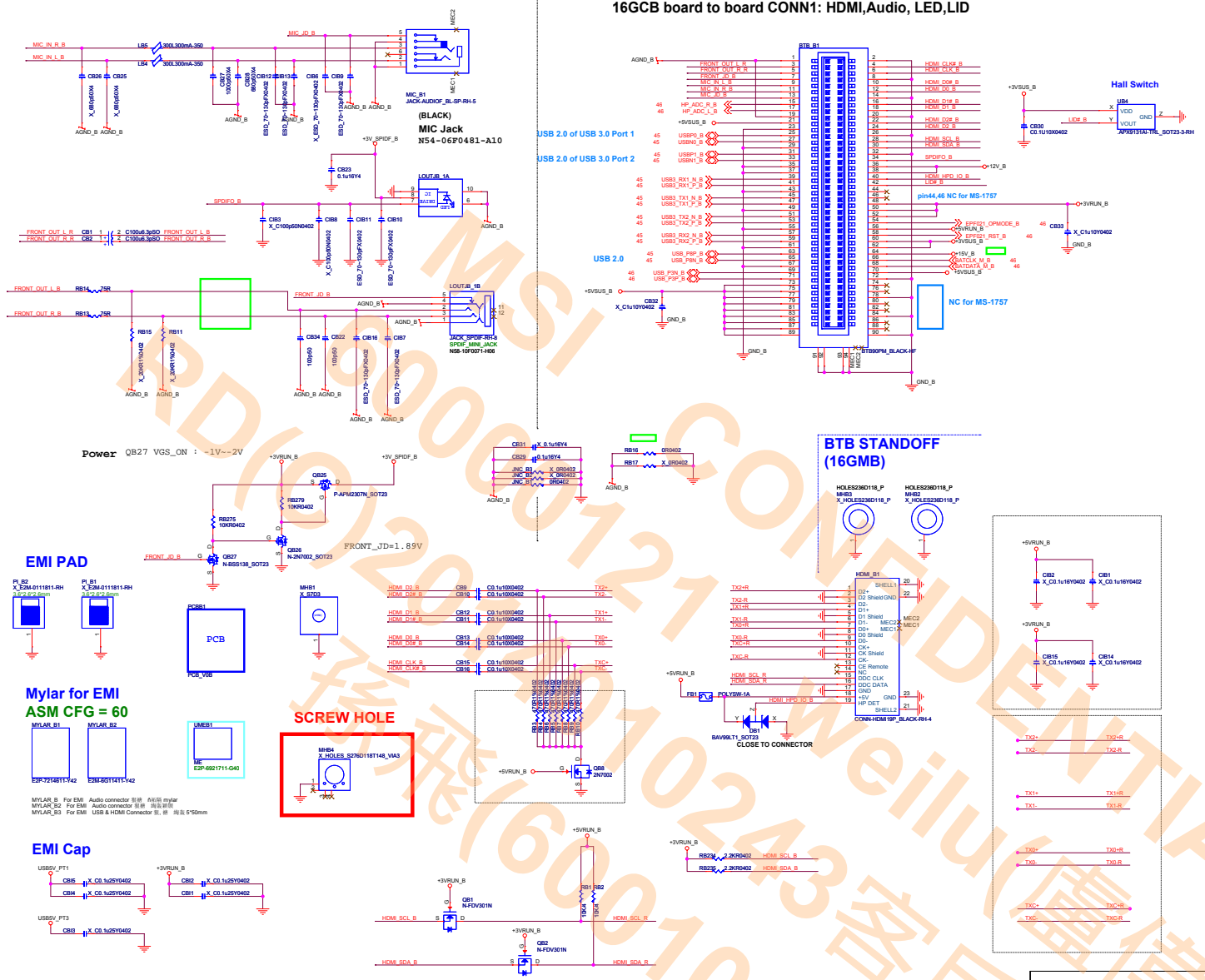
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Rev	1.0	MS 16GE	11

GIGA LAN(BFN2200A)



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Size	Document Number	Rev	
Custom	MS 16GE	11	
Date	Expire	Sheet	of
2014-03-03	2014	43	60

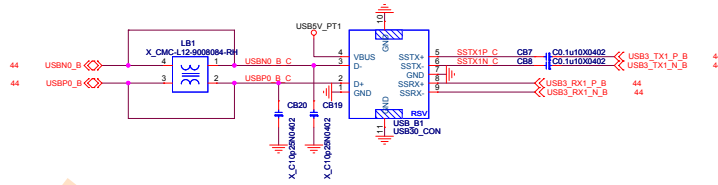
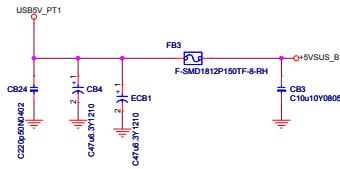
16GCB board to board CONN1: HDMI,Audio, LED,LID



File: [B] BTR CNT/Audio/HDMI
Size: Document Number: Rev: 11
Custom: MS_16GF
Date: Friday, January 03, 2014 Sheet: 44 of 50

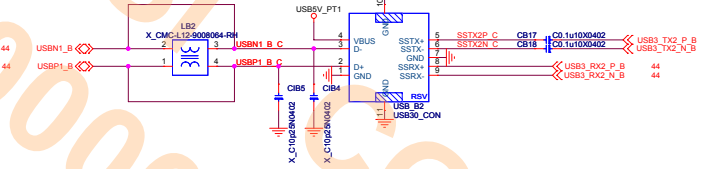
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(USB3.0 Left Side - UP)



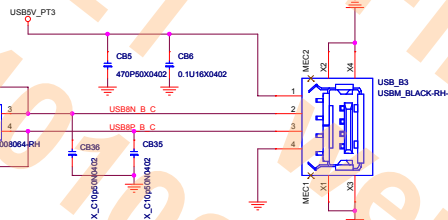
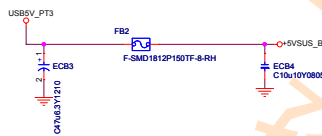
USB 3.0 CNT 2

(USB3.0 Left Side - Down)



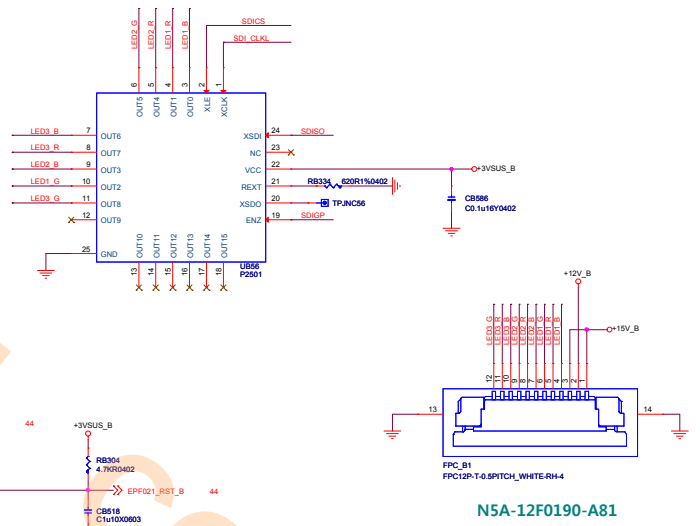
USB 2.0 CNT

(Left Side)



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Sheet	11
Class	MS 16GE
Issue	1.000 2014.03.20
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LED 8051 Controller



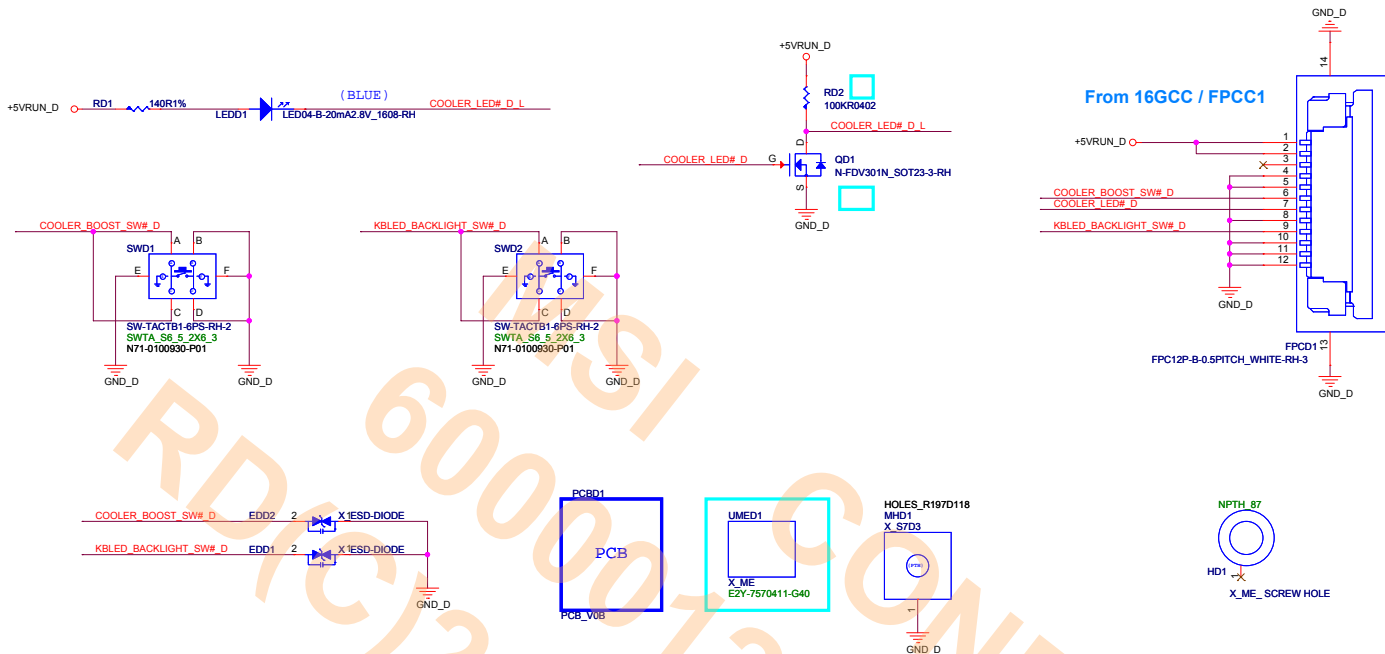
N5A-12F0190-A81

LED Keyboard

For EMI

- CB853 X C100p50N0402 LED1_G
- CB854 X C100p50N0402 LED1_R
- CB855 X C100p50N0402 LED1_B
- CB856 X C100p50N0402 LED2_G
- CB857 X C100p50N0402 LED2_R
- CB858 X C100p50N0402 LED2_B
- CB859 X C100p50N0402 LED3_G
- CB860 X C100p50N0402 LED3_R
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- CB865 X C100p50N0402 LED5_G
- CB866 X C100p50N0402 LED5_R
- CB867 X C100p50N0402 LED5_B
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- CB870 X C100p50N0402 LED6_B
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- CB873 X C100p50N0402 LED7_B
- CB874 X C100p50N0402 LED8_G
- CB875 X C100p50N0402 LED8_R
- CB876 X C100p50N0402 LED8_B
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- CB1076 X C100p50N0402 LED75_R
- CB1077 X C100p50N0402 LED75_B
- CB1078 X C100p50N0402 LED76_G
- CB1079 X C100p50N0402 LED76_R
- CB1080 X C100p50N0402 LED76_B
- CB1081 X C100p50N0402 LED77_G
- CB1082 X C100p50N0402 LED77_R
- CB1083 X C100p50N0402 LED77_B
- CB1084 X C100p50N0402 LED78_G
- CB1085 X C100p50N0402 LED78_R
- CB1086 X C100p50N0402 LED78_B
- CB1087 X C100p50N0402 LED79_G
- CB1088 X C100p50N0402 LED79_R
- CB1089 X C100p50N0402 LED79_B
- CB1090 X C100p50N0402 LED80_G
- CB1091 X C100p50N0402 LED80_R
- CB1092 X C100p50N0402 LED80_B
- CB1093 X C100p50N0402 LED81_G
- CB1094 X C100p50N0402 LED81_R
- CB1095 X C100p50N0402 LED81_B
- CB1096 X C100p50N0402 LED82_G
- CB1097 X C100p50N0402 LED82_R
- CB1098 X C100p50N0402 LED82_B
- CB1099 X C100p50N0402 LED83_G
- CB1100 X C100p50N0402 LED83_R
- CB1101 X C100p50N0402 LED83_B
- CB1102 X C100p50N0402 LED84_G
- CB1103 X C100p50N0402 LED84_R
- CB1104 X C100p50N0402 LED84_B
- CB1105 X C100p50N0402 LED85_G
- CB1106 X C100p50N0402 LED85_R
- CB1107 X C100p50N0402 LED85_B
- CB1108 X C100p50N0402 LED86_G
- CB1109 X C100p50N0402 LED86_R
- CB1110 X C100p50N0402 LED86_B
- CB1111 X C100p50N0402 LED87_G
- CB1112 X C100p50N0402 LED87_R
- CB1113 X C100p50N0402 LED87_B
- CB1114 X C100p50N0402 LED88_G
- CB1115 X C100p50N0402 LED88_R
- CB1116 X C100p50N0402 LED88_B
- CB1117 X C100p50N0402 LED89_G
- CB1118 X C100p50N0402 LED89_R
- CB1119 X C100p50N0402 LED89_B
- CB1120 X C100p50N0402 LED90_G
- CB1121 X C100p50N0402 LED90_R
- CB1122 X C100p50N0402 LED90_B
- CB1123 X C100p50N0402 LED91_G
- CB1124 X C100p50N0402 LED91_R
- CB1125 X C100p50N0402 LED91_B
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- CB1127 X C100p50N0402 LED92_R
- CB1128 X C100p50N0402 LED92_B
- CB1129 X C100p50N0402 LED93_G
- CB1130 X C100p50N0402 LED93_R
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- CB1136 X C100p50N0402 LED95_R
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- CB1139 X C100p50N0402 LED96_R
- CB1140 X C100p50N0402 LED96_B
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- CB1142 X C100p50N0402 LED97_R
- CB1143 X C100p50N0402 LED97_B
- CB1144 X C100p50N0402 LED98_G
- CB1145 X C100p50N0402 LED98_R
- CB1146 X C100p50N0402 LED98_B
- CB1147 X C100p50N0402 LED99_G
- CB1148 X C100p50N0402 LED99_R
- CB1149 X C100p50N0402 LED99_B
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- CB1151 X C100p50N0402 LED100_R
- CB1152 X C100p50N0402 LED100_B

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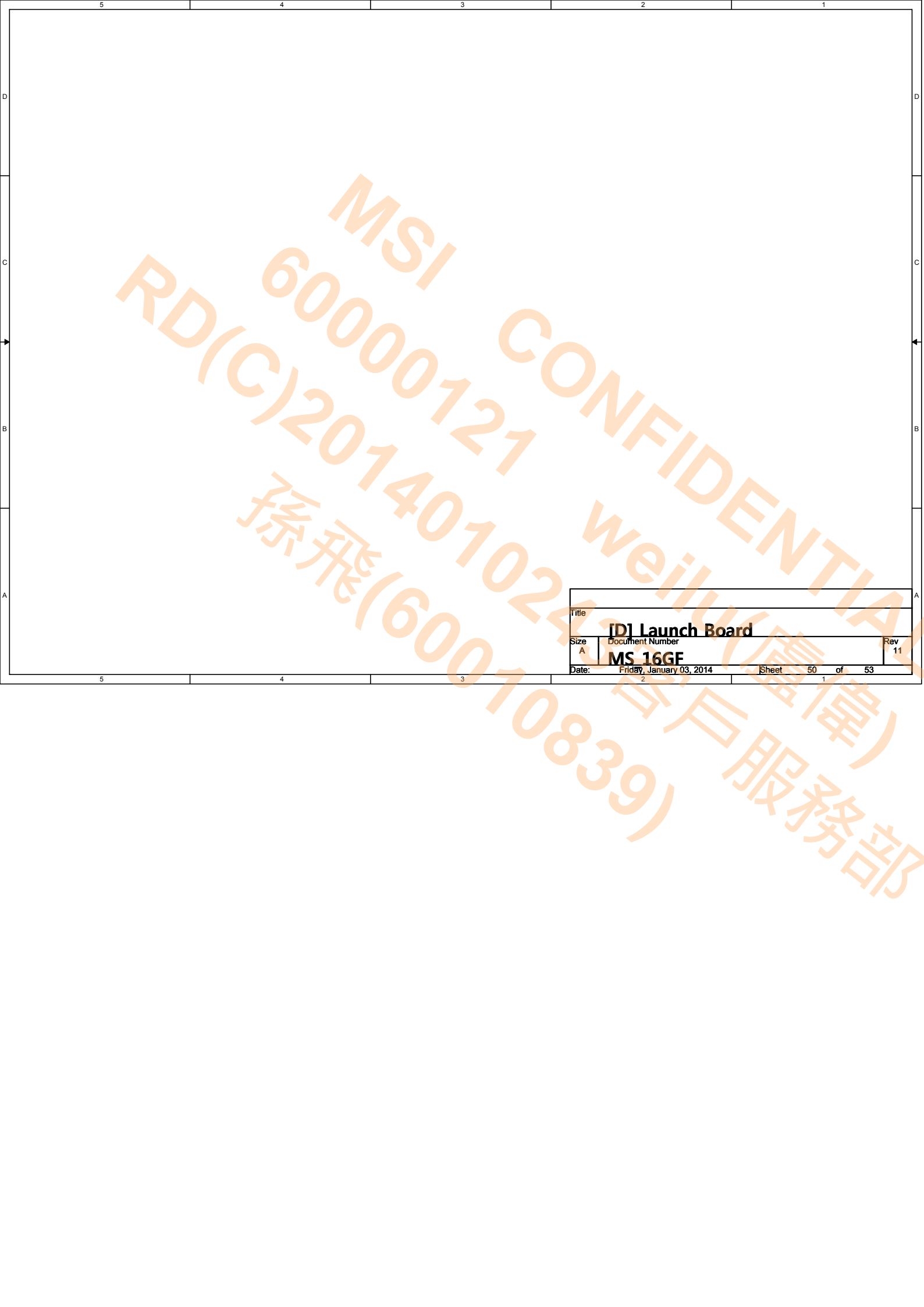
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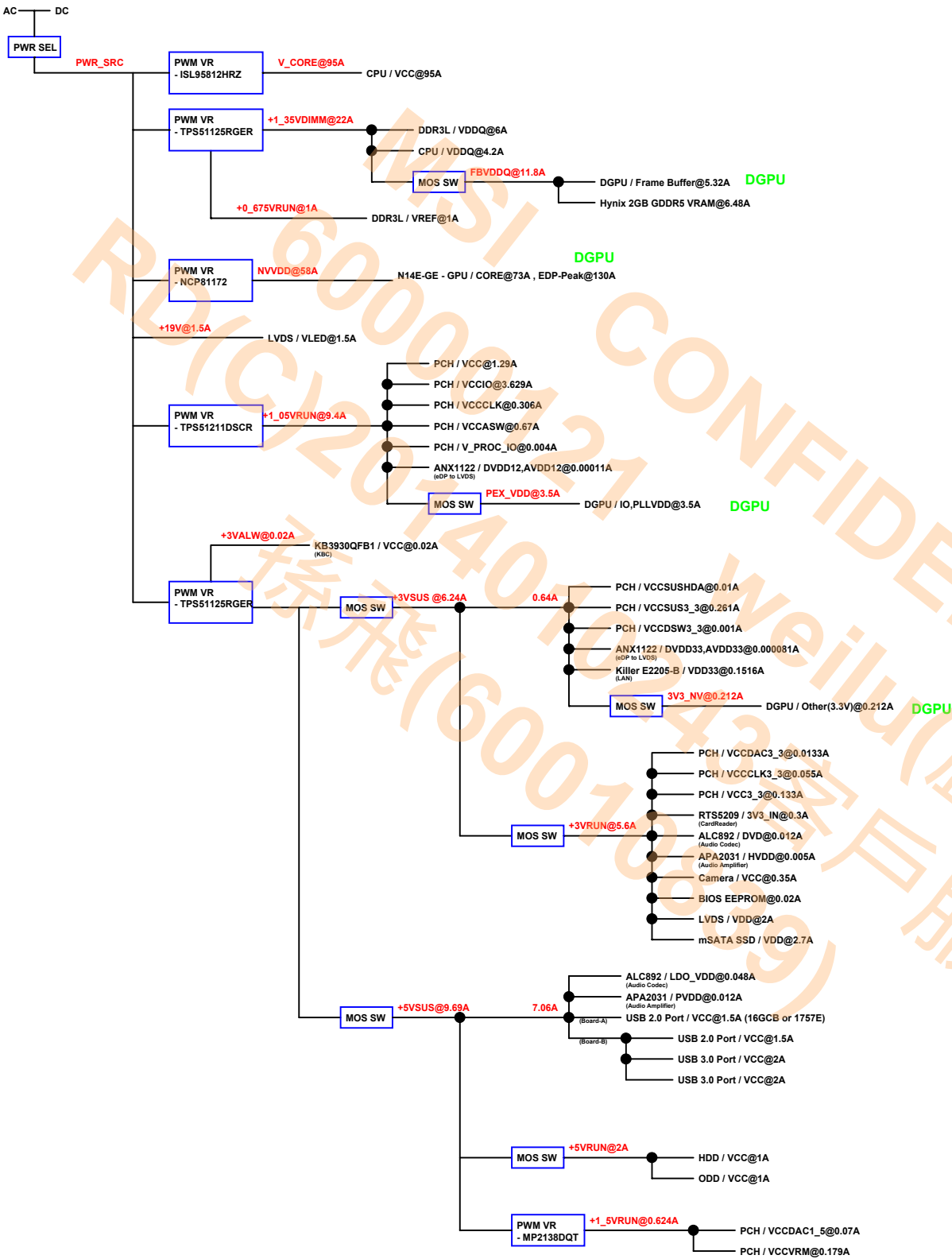
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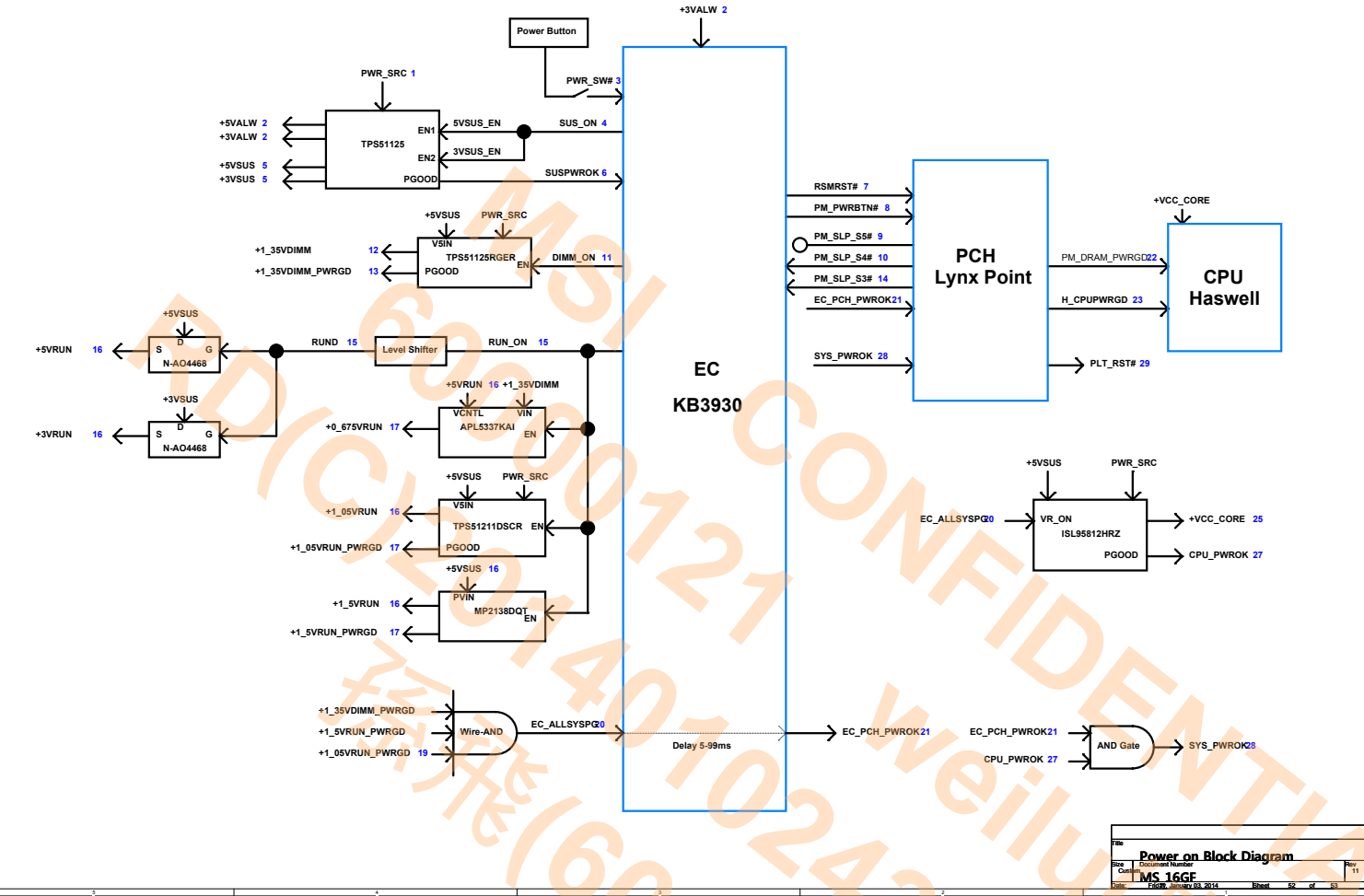


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1757 Power Delivery Chart

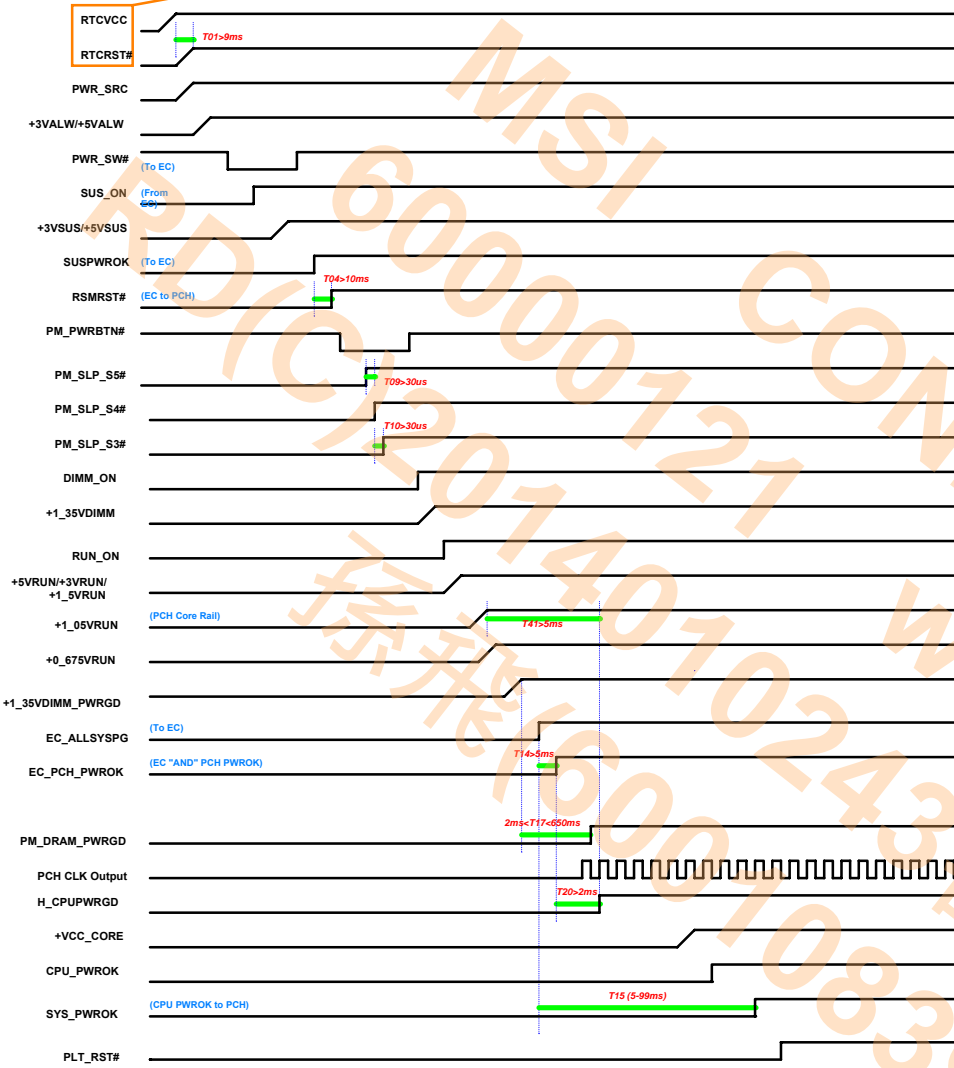


1757 Power on Block Diagram



Power on Sequence

G3 -> S0



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